CURRICULUM AND SYLLABUS (R2015)
CHOICE BASED CREDIT SYSTEM

M.TECH. APPLIED ELECTRONICS
(FULL TIME)
I – IV SEMESTERS

SEMESTER-I						
Sub Code	**Category**	**Subject Name**	**L**	**T**	**P**	**C**
Theory						
MMA101	PM	Applied Mathematics for Electronics Engineers	3	2	0	4
MAE101	PC	Statistical Signal Processing	3	0	0	3
MAE102	PC	Advanced Digital System Design	3	0	0	3
MVD102	PC	Introduction to VLSI Design	3	0	0	3
MAE1E1	PE	Professional Elective-I	3	0	0	3
Practical						
MAE1L1	PC	Advanced Electronics system Design Lab-I	0	0	4	2
Total No. of Contact Hours: 21					**Total Credits:18**	

SEMESTER-II						
Sub Code	**Category**	**Subject Name**	**L**	**T**	**P**	**C**
Theory						
MAE201	PC	Analysis and Design of Analog Integrated circuits	3	0	0	3
MAE202	PC	Computer Architecture and Parallel Processing	3	0	0	3
MAE203	PC	Digital Image Processing	3	0	0	3
MAE2E2	PE	Professional Elective-II	3	0	0	3
MAE2E3	PE	Professional Elective-III	3	0	0	3
Practical						
MAE2L2	PC	Advanced Electronics system Design lab-	0	0	4	2

		II				
Total No. of Contact Hours: 21					**Total Credits: 17**	

SEMESTER-III						
Sub Code	**Category**	**Subject Name**	**L**	**T**	**P**	**C**
Theory						
MAE3E4	PE	Professional Elective-IV	3	0	0	3
MAE3E5	PE	Professional Elective-V	3	0	0	3
MAE3E6	OE	Open Elective - I	3	0	0	3
MAE3P1	PR	Project work phase-I	0	0	12	6
Total No. of Contact Hours: 22					**Total Credits:15**	

SEMESTER-IV						
Sub Code	**Category**	**Subject Name**	**L**	**T**	**P**	**C**
MAE4P2	PR	Project work phase-II	0	0	24	12
Total No. of Contact Hours: 24					**Total Credits: 12**	

OVERALL CREDIT OF THE PROGRAMME – 62

LIST OF ELECTIVES

PROFESSIONAL ELECTIVE – I (PE-I)

Code No.	Course Title	L	T	P	C
MAE001	Design and Analysis of Algorithms	3	0	0	3
MAE002	Robotics	3	0	0	3
MAE003	RF System design	3	0	0	3

PROFESSIONAL ELECTIVE – II (PE-II)

Code No.	Course Title	L	T	P	C

MAE005	Advanced Microprocessors and Microcontrollers	3	0	0	3
MAE006	High Speed Switching Architectures	3	0	0	3
MAE 013	Blue Tooth Technology	3	0	0	3

PROFESSIONAL ELECTIVE – III (PE-III)

Code No.	Course Title	L	T	P	C
MAE101	Advanced Digital Signal Processing	3	0	0	3
MAE004	Electromagnetic Interference and Compatibility in System Design	3	0	0	3
MVL010	Optimization Techniques In VLSI Design	3	0	0	3

PROFESSIONAL ELECTIVE – IV (PE-IV)

Code No.	Course Title	L	T	P	C
MAE 015	High Performance communication networks	3	0	0	3
MAE 014	Internet Working Multimedia	3	0	0	3
MAE 011	VLSI SIGNAL PROCESSING	3	0	0	3

PROFESSIONAL ELECTIVE – V (PE-V)

Code No.	Course Title	L	T	P	C
MAE004	DSP Integrated systems	3	0	0	3
MAE 009	Low power VLSI Design	3	0	0	3
MAE 010	Analog VLSI Design	3	0	0	3

OPEN ELECTIVE – I(OE-I)

Code No.	Course Title	L	T	P	C
MED102	EMBEDDED SYSTEMS	3	0	0	3
MED201	ASIC DESIGN	3	0	0	3
	Research Methodology	3	0	0	3

SUMMARY OF CURRICULUM STRUCTURE AND CREDIT & CONTACT HOUR DISTRIBUTION

S. No.	Sub Area	Credit AS per Semester				No. of Credit	% of credit
		I	II	III	IV		
1	Professional Mathematics (PM)	4				4	6.06
2	Professional Core (PC)	12	12			24	36.36
3	Professional Electives (PE)	3	6	6		15	22.72
4	Open Electives (OE)			3		3	4.54
5	Project Work, Seminar, Internship, Term Paper, etc. (PR)			6	12	20	30.30
6	Total Credit	18	17	15	12	62	100
7	Total Contact Hour	21	21	22	24	88 Hrs	-

Course Code MMA101	Course Name: APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS	L	T	P	C
	Total Contact Hours:60	3	1	0	4
	Prerequisite: ENGINEERING MATHEMATICS				
	Course Designed by : Dept of Mathematics				

OBJECTIVES

To apply all taught techniques to unseen problems, and queuing is a major branch of optimization, Random variable compute and interpret means, correlation/covariance, PERT and CPM chart is mainly used for documenting the data(visually) on projects.

COURSE OUTCOMES (COs)

CO1	The student will learn to analyse and solve the fundamental problems with prescribed conditions in simple cases.
CO2	The student will learn to understand how signals, systems, inference combine in prototypical tasks of communication.
CO3	The student will learn to manipulate matrices and to do matrix algebra, determinants, eigen values Eigen vectors and to solve the system of linear equations.
CO4	The student will learn to understand how signals, systems, control.
CO5	The student will learn to understand how signals, systems, signal processing.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1	H				
	CO2		M			
	CO3	H				
	CO4			M		
	CO5				L	
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I ONE DIMENSIONAL RANDOM VARIABLES 12

Random variables and their functions - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Exponential, Gamma, Weibull and Normal distributions.

UNIT II MATRIX THEORY 12

Eigen values using QR Transformations generalized eigenvectors – Canonical forms, singular valued composition and application – matrix norms and induced norms Psuedo inverse – least square approximations

UNIT III SPECIAL FUNCTIONS 12

Bessel's Equation- Bessel Functions- Legendre's Equation- Legendre Polynomials- Rodrigue's Formula- Recurrence Relations- Generating Functions and Orthogonal Property for Bessel Function of the First Kind.

UNIT IV OPERATIONS RESEARCH 12

Network Definitions – Minimal Spanning Tree algorithm – Shortest Route Problem – Maximal Flow model – Minimum Cost Capacitated Flow Problem – CPM and PERT.

UNIT V QUEUING THEORY 12

Single and Multiple Server Markovain Queuing Models – Customer Impatience Priority Queues M/g / I Queuing System –Queuing Applications.

TEXT BOOKS:

1. Handy A.Taha., "Operations Research An Introduction", 7th Edn. Pearson Education , Chennai-113. 2002.
2. Donald Gross and Carl M. Harris, "Fundamentals of Queuing Theory", 2nd Edn.
3. Wiley India Pvt Ltd, New Delhi.

REFERENCE BOOKS:

1. Freund J.D. and Miller JR "Probability Statistics for Engineers" Prentice Hall of India, 5th Edition, New Delhi. 1994.
2. Gupta.SC and Kapoor V.K. "Fundamentals of Mathematics Statistics" Sultan Chand & Sons, New Delhi.
3. Stewart G.W. "Introduction to Matrix Computaions" Academic Press, New York.

Course Code MAE103	**Course Name: STATISTICAL SIGNAL PROCESSING**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Digital Signal Processing				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES:

To Introduce the basics of random signal processing and Concept wise Introduction to Estimation and prediction theory.

COURSE OUTCOMES (COs)

CO1	Students will analyze the random signal processing
CO2	Students will learn to understand the speech signal processing
CO3	Students will develop knowledge in Estimation and Prediction theory.
CO4	To know about adaptive filtering and its Applications.
CO5	A brief overview of the processing of speech signals.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	e
2	CO1	H				
	CO2		M			
	CO3			H		L
	CO4	H			M	
	CO5		H			
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I INTRODUCTION TO RANDOM SIGNAL PROCESSING 9

Discrete Random Processes- Ensemble Averages, Stationary processes, Bias and Estimation, Autocovariance, Autocorrelation, Parseval's theorem, Wiener-Khintchine relation, White noise, Power Spectral Density, Spectral factorization, Filtering Random Processes, Special types of Random Processes – ARMA, AR, MA – Yule-Walker equations.

UNIT II SPECTRAL ESTIMATION 9

Estimation of spectra from finite duration signals, Nonparametric methods - Periodogram, Modified periodogram, Bartlett, Welch and Blackman-Tukey methods, Parametric method, AR (p) spectral estimation and detection of Harmonic signals, MUSIC algorithm.

UNIT III LINEAR ESTIMATION AND PREDICTION 9

Linear Prediction of Signals-Forward and Backward Predictions, Solution to Prony's normal equation, Levinson Durbin Algorithm, Lattice filter realization of prediction error filters. Linear Minimum Mean-Square Error (LMMSE)

UNIT IV ADAPTIVE FILTERS 9

FIR adaptive filters – adaptive filter based on steepest descent method- Widrow-Hopf LMS algorithm, Normalized LMS algorithm, Adaptive channel equalization, Adaptive echo cancellation, Adaptive noise cancellation, RLS adaptive algorithm.

UNIT V APPLICATION OVERVIEW-SPEECH PROCESSING 9

Speech Fundamentals: Articulatory Phonetics – Production and Classification of Speech Sounds; Acoustic Phonetics – acoustics of speech production; Short-term Fourier transform (STFT): overview of Fourier representation, non-stationary signals, development of STFT, transform and filter-bank views of STFT; Short time Homomorphic Filtering of Speech; Linear Prediction (LP) analysis: Basis and development, Levinson-Durbin's method, normalized error, LPC spectrum.

TEXT BOOKS:

1. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley and Sons, Inc, Singapore, 2002.
2. Lawrence Rabiner and Biing-Hwang Juang, "Fundamentals of Speech Recognition",

REFERENCE BOOKS:

1. Pearson Education, 2003.
2. Dimitris G. Manolakis and Vinay K .Ingle ,"Applied Digital Signal Processing", Cambridge University Press, 2011.
3. L.R. Rabiner and R.W. Schafer, "Introduction to Digital Speech Processing" (Foundations and Trends in Signal Processing), Now Publishers Inc., USA, 2007.

Course Code MAE102	**Course Name: ADVANCED DIGITAL SYSTEM DESIGN**	**L**	**T**	**P**	**C**
	Total Contact Hours: 60	3	1	0	4
	Prerequisite: Digital communication				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To learn the concepts of theorems and other techniques to design minimized logic functions and To Understand the concepts of synchronous and asynchronous sequential circuit design and

COURSE OUTCOMES (COs)

CO1	Ability to analyze and design sequential digital circuits
CO2	Ability to understand the requirements and specifications of the system required for a given application
CO3	Ability to understand programmable logic devices
CO4	To learn about the faults in logic circuits and metods of diagnoising it
CO5	To learn about programmable logic devices.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E

2	CO1		M			
	CO2	H				
	CO3	H				
	CO4		M			
	CO5			L		
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I ADVANCED TOPICS IN BOOLEAN ALGEBRA **9**

Shannon's expansion theorem, Consensus theorem, Octal designation, Run measure, INHIBIT/INCLUSION/AOI/Driver /Buffer gates ,Gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method ,Design of static hazard free and dynamic hazard free logic circuits.

UNIT II STNCHRONOUS SEQUENTIAL CIRCUIT DESIGN **9**

Analysis of clocked synchronous sequential Networks (CSSN), Modeling of CSSN,State table assignment and reduction, Design of CSSN,Design of iterative circuit, ASM Chart, ASM Realization. Design of Arithmetic circuits for Fast adder,Array Multiplier.

UNIT III ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN **9**

Analysis of Asynchronous Sequential Circuit (ASC) ,Flow Table Reduction , Races in ASC , State Assignment Problem and the Transition Table, Design of ASC ,Data Synchronizers, Designing vending Machine Controller, Mixed Operating Mode Asynchronous Circuits.

UNIT IV FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS **9**

Fault Table Method ,Path Sensitization Method, Boolean Difference Method,Kohavi Algorithm, Tolerance Techniques , The Compact Algorithm,Practical PLA"s, Fault in PLA Circuit Test Approach, Transition Check Approach , State identification and fault detection experiment .

UNIT-V PROGRAMMMABLE LOGIC DEVICES **9**

Basic concepts, Programming technologies, Programmable Logic element(PLE),Programmable Logic Array(PLA),System Design using PLD's-Design of

combinational and sequential circuits using PLD's(CPLD).Programming PAL device using PALSAM ,Design of state machine using Algorithmic State Machines (ASM) chart as a design tool, Introduction to Field Programmable Gate Arrays –Types of FPGA, Xilinx XC 3000 series, Logic Cell Array (LCA),Configurable Logic Blocks(CLB) INPUT/OUTPUT Block(IPB)-Programmable Interconnect Point (PIP),Introduction to Actel AACT2 FAMILY AND XILINX XC 4000 families ,Design examples.

TEXT BOOK:

1. William I.Flectcher, "An Engineering Approach to Digital Design", PrenticeHall of India.
2. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
3. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
4. Digital Circuits and Logic Design – Samuel C. Lee , PHI

REFERENCES BOOK:

1. Donald G. Givone, "Digital principles and Design", Tata McGraw Hill 2002.
2. Parag K Lala, "Digital System design using PLD", BS Publications, 2003.
3. John M Yarbrough, "Digital Logic applications and Design", Thomson Learning, 2001.
4. Nripendra N Biswas, "Logic Design Theory", Prentice Hall of India, 2001.
5. Charles H. Roth Jr., "Fundamentals of Logic design", Thomson Learning, 2004.

Course Code MVL102	**Course Name: INTRODUCTION TO VLSI DESIGN**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Basic VLSI Design				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To understand the concepts of MOS transistors operations and their AC , DC Characteristics and To know the fabrication process of CMOS technology and its layout design rules and To know the concepts of power estimation and delay calculations in cmos circuits

COURSE OUTCOMES (COs)

CO1	To learn the basic MOS and CMOS circuit, characteristics and performance.
CO2	To learn the circuit components at physical level design.
CO3	To learn the different abstract levels in Verilog for modeling digital circuits.
CO4	To learn about the VLSI circuit components and physical design
CO5	To study the concepts of Verilog in designing digital logic circuits.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2	L				
	CO3			L		
	CO4		M			

	CO5		H			
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT – I MOS TECHNOLOGY AND CIRCUITS **9**

MOS Technology and VLSI, Process parameters and consideration for BJT, MOS and CMOS, CMOS logic, MOS transistor theory , Enhancement mode transistor action, Ideal I-V characteristics, DC transfer characteristics, Threshold voltage, Body effect,Design equations, Second order effects. MOS models and small signal AC characteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance model

UNIT –II CMOS CIRCUITS DESIGN PROCESS **9**

CMOS fabrication, P -Well process, N -Well process, twin - tub process, MOS layers stick diagrams and Layout diagram, Layout design rules, Latch up in CMOS circuits, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION **9**

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT – IV **VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN** 9

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits, Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modelling, cross talk, floor planning, power distribution ,Clock distribution.

UNIT V SPECIFICATION USING VERILOG HDL **9**

Basic concepts- identifiers- gate primitives, gate delays, operators, timing controls, procedural assignments conditional statements, Data flow and RTL, structural gate level switch level modeling, Design hierarchies, Behavioral and RTL modeling, Test benches, Design of decoder, equality detector, comparator, priority encoder, half adder, full adder, Ripple carry adder, D latch and D flip flop

TEXT BOOK:

1. Douglas A. Pucknell and Kamran Eshraghian, “Basic VLSI Design Systems and Circuits”, Prentice Hall of India Pvt. Ltd., 1993.

2. Wayne Wolf, "Modern VLSI Design", 2nd Edition, Prentice Hall 1998.
3. Amar Mukherjee, "Introduction to NMOS and CMOS VLSI System Design," Prentice Hall,

REFERENCES BOOK:

1 . John P.Uyemura "Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc.,2002..
2 Fabricious E. "Introduction to VLSI Design", McGraw Hill, 1990.
3 J.Bhasker: Verilog HDL primer, BS publication,2001
4. Ciletti Advanced Digital Design with the Verilog HDL, Prentice Hall of India, 2003

Course Code MAE1L1	**Course Name: ADVANCED ELECTRONICS SYSTEM DESIGN LAB-1**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	0	0	4	2
	Prerequisite: ELECTRONICS SYSTEM DESIGN				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES :

- To design digital circuits using Hardware Description languages and to learn about SPICE simulation

COURSE OUTCOMES (COs)

CO1	Design and test digital logic circuits on FPGA.
CO2	Design Electronic circuits using SPICE and PCB layout using EDA tools
CO3	To learn about the design of digital circuits of MULTIPLEXER, DEMULTIPLEXER using Hardware description languages
CO4	To learn about the design of digital circuits of ENCODER, DECODER using Hardware description languages
CO5	To learn about the design of digital circuits of JK, D, T, SR FLIPFLOPS

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	e
2	CO1		H			
	CO2	M			L	
	CO3			H		
	CO4		H			L
	CO5	M			M	

3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

(EXPERIMENTS FROM 1 TO 6 SHOULD BE DONE USING VERILOG VHDL ON FPGA)

1. DESIGN AND TESTING OF HALF ADDER, FULL ADDER.
2. DESIGN AND TESTING OF HALF SRACTOR/FULL SUBTRACTOR.
3. DESIGN AND TESTING OF JK, D, T, SR FLIPFLOPS.
4. DESIGN AND TESTING OF COUNTERS.
5. DESIGN AND TESTING OF MULTIPLEXER, DEMULTIPLEXER.
6. DESIGN AND TESTING OF MAGNITUDE COMPARATOR WITH 8 BITS.
7. DESIGN AND TESTING OF ELECTRONICS CIRCUITS USING SPICE SIMULATION (HARTELY OSCILATOR /COLPITTS OSCILATOR AND RC-COUPLED AMPLIFIER)
8. SCHEMATIC CAPTURE & PCB LAYOUT DESIGN USING EDA TOOLS LIKE ORCAD

Course Code MAE201	**Course Name: ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Linear Integration Circuits				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To design the single stage amplifiers using pmos and nmos driver circuits with different loads and analyse high frequency concepts of single stage amplifiers and noise characteristics associated v differential amplifiers

COURSE OUTCOMES (COs)

CO1	Ability to analyse the design of single and two stage operational amplifiers and voltage references, and determine the device dimensions of each MOSFETs involved.
CO2	To understand the design techniques of switched capacitor filters
CO3	To study the different types of current mirrors
CO4	To know the concepts of voltage and current reference circuits
CO5	To understand about MOS switched capacitor filters.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2		M			
	CO3	H			M	
	CO4		M			L
	CO5			L		
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT-I CIRCUIT CONFIGURATION FOR LINEAR IC **9**

Current source, analysis of difference amplifiers with active load, Supply and temperature independent biasing techniques, voltage references.

UNIT-II OPERATIONAL AMPLIFIERS **9**

Analysis of operational amplifier circuits, slew rate model and high frequency analysis, operational amplifier noise analysis and low noise operational amplifiers.

UNIT-III ANALOG MULTIPLIER AND PLL **9**

Analysis of MOS operational Amplifier, CMOS voltage references, MOS Power amplifier and analog switches.

UNIT-IV MOS ANALOG ICS **9**

Design of MOS Operational Amplifier,CMOS Voltage references,MOS power amplifier and analog switches.

UNIT-V MOS SWITCHED CAPACITOR FILTERS **9**

Design techniques for switched capacitor filter, CMOS switched capacitor filters, MOS integrated active RC filters.

TEXT BOOK:

1. Kenneth R.Laker, Willy M.C.Sansen, William M.C.Sansen, "Design of Analog Integrated Circuits and Systems ", McGraw Hill, 1994.
2. Behzad Razavi, "Principles of Data Conversion System Design", S.Chand &Company ltd, 2000.

REFERENCES BOOK:

1. Gray and Meyer, "Analysis and Design of Analog IC's, Wiley International, 1996.

2. Gray, Wooley, Broderson, “Analog MOS Integrated Circuits”, IEEE Press 1989.

Course Code MAE202	Course Name: COMPUTER ARCHITECTURE AND –PARALLEL PROCESSING	L	T	P	C
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Computer Architecture				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To understand the difference between the pipeline and parallel concepts and To study the various types of architectures and the importance of scalable architectures and To study the various memories and optimization of memory.

COURSE OUTCOMES (COs)

CO1	At the end of the course, the student will be able to:
CO2	Compare and evaluate the performance of various architectures.
CO3	Design sub-systems to meet specific performance requirements
CO4	Analyze the requirements of large systems to select and build the right infrastructure.
CO5	To study the various memories and optimization of memory.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2	H		M		
	CO3		H			
	CO4		M		M	
	CO5		H			L
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT-I THEORY OF PARALLESISM –PART-I

7

Parallel computer models-the state of computing, Multiprocessor and Multicomputer and Multivectors and SIMD computers, PRAM and VLSI mode Architectural development tracks .Program and properties Conditions of parallelism.

UNIT-II THEORY OF PARALLELISM –PART-II

10

Program partitioning and scheduling, Program flow mechanism, System inter connect architecture, Principles of scalable performance–performance matrices and measures, Parallel processing application speedup performance laws, scalability analysis and approaches.

UNIT-III HARDWARE TECHNOLOGIES

10

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory-backplane bus systems, cache memory organizations, shared memory organization, sequential and weal consistency model.

UNIT-IV PIPELINING AND SUPERSCALAR TECHNOLOGIES

10

Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivectors and SSIMD Computers, Scalable Multithread and dataflow architectures.

UNIT-V SOFTWARE AND PARALLEL PROCESSING

10

Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

TEXT BOOK:

1. Kai Hawang, "Advanced Computer Architecture", McGraw Hill international, 1993.

REFERENCES BOOK:

1.William Stallings, "Computer Organization and Architecture", Macmillan Publishing Company, 1990.

2. M.J.Quinn, "Designing Efficient Algorithms for Parallel Computer", McGraw Hill International1994.

Course Code MAE203	**Course Name: DIGITAL IMAGE PROCESSIN(**	**L**	**T**	**P**	**C**
	Total Contact Hours: 60	3	1	0	4
	Prerequisite: Digital Signal Processing				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES :

To understand techniques for image enhancement and to understand techniques for image segmentation.

COURSE OUTCOMES (COs)

CO1	To be able to design and implement image enhancement schemes.
CO2	To be able to design and implement compression schemes.
CO3	To be able to design and implement restoration schemes.
CO4	To be able to design and implement segmentation schemes
CO5	To understand techniques for image compression

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	e
2	CO1	H			M	
	CO2		H			

	CO3	H		M	M	
	CO4		H			L
	CO5			M		
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I IMAGE REPRESENTATION **9**

Image representation-Image Basis Functions- Two dimensional DFT- Discrete Cosine Transform-Walsh- Hadamard transform-Wavelet transform- Principal component analysis.

UNIT II IMAGE ENHANCEMENT AND RESTORATION 9

Gray level transformation techniques- Spatial domain techniques - Half toning, Median filtering, contrast stretching, Histogram Equalization- Frequency domain techniques - Weiner filtering-Homomorphic filtering- PSFs for different forms of blur - noise models- color image processing.

UNIT III IMAGE SEGMENTATION **9**

Segmentation - Similarity and dissimilarity methods- Thresholding - Edge based and Region based methods- Hough transform- Morphological operations - Clustering methods.

UNIT IV IMAGE COMPRESSION **9**

Source coding techniques - Run length coding - Shannon-Fano coding- Huffman coding- Arithmetic coding- LZW coding - Transform and Predictive compression methods - Vector quantization- case studies - JPEG-MPEG.

UNIT V SIMULATION **9**

Implementation of Image processing algorithms - Image Enhancement - Restoration- Segmentation-Coding techniques- Applications.

TEXT BOOKS:

1. Gonzalez R. C. and Woods R.E., "Digital Image Processing", 3rd Edition, Prentice-Hall, 2008.
2. Jain A.K., "Fundamentals of Digital Image Processing", PHI Learning Private Ltd., 1989.
3. William K. Pratt, "Digital Image Processing", John Wiley, 4th Edition, 2007.

REFERENCES BOOKS:

1. Sonka M, "Image Processing, Analysis and Machine Vision", Vikas Publishing

Home (Thomson) 2001.
2. Schalkoff R.J., "Digital Image Processing & Computer Vision", John Wiley & Sons, 1992. 6. Richard O. Duda, Peter E. Hart and David G. Stork., "Pattern Classification", Wiley, 2001.
3. J.W. Woods, "Multidimensional Signal, Image, Video Processing and Coding", 2nd Edition, Academic Press, 2012.

Course Code MAE2L2	Course Name: ADVANCED ELECTRONI SYSTEM DESIGN LAB-II LIST OF EXPERIMENTS	L	T	P	C
	Total Contact Hours:45	0	0	4	2
	Prerequisite: Advanced Electronics System Design Lab-I				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To learn about pic microcontroller.

COURSE OUTCOMES (COs)

CO1	Students will learn about the interfacing concepts and implement it by using PIC microcontroller.
CO2	Students will learn about the interfacing concepts and implement it by using stepper motor interface
CO3	Students will learn about the traffic light controller interfacing concepts and implement it by using PIC microcontroller
CO4	Students will learn about the Dac / Dc Motor Speed Controller interfacing concepts and implement it by using PIC microcontroller
CO5	Students will learn about the Pic To Serial (Rs232) Communication interfacing concepts and implement it by using PIC microcontroller

Mapping of Course Outcomes with Program outcomes (POs)

(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	e
2	CO1					
	CO2	H			H	
	CO3		M			
	CO4			M		M
	CO5		L		M	

3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

(EXPERIMENTS FROM 1 TO 6 SHOULD BE DONE USING PIC MICROCONTROLLER)

1. ADC INTERFACE WITH TEMPERATURE SENSOR
2. STEPPER MOTOR INTERFACE
3. TRAFFIC LIGHT CONTROLLER
4. DAC / DC MOTOR SPEED CONTROLLER
5. PIC TO SERIAL (RS232) COMMUNICATION
6. 5X7 MATRIX LED DISPLAY INTERFACE AND 16X2 CHARACTER LCD INTERFACE
7. DESIGN OF SMPS
8. DESIGN OF INVERTER.

ELECTIVES

Course Code	**Course Name: DESIGN AND ANALYSIS OF ALGORITHMS**	**L**	**T**	**P**	**C**
MAE001	Total Contact Hours:45	3	0	0	3
	Prerequisite: Analysis Of Algorithms				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

- Discusses the algorithmic complexity parameters and the basic algorithmic design techniques.
- To discuss the graph algorithms, algorithms for NP Completeness Approximation Algorithms and NP Hard Problems.

COURSE OUTCOMES (COs)

CO1	Will be able to apply the suitable algorithm according to the given optimization problem.

CO2	Ability to modify the algorithms to refine the complexity parameters.
CO3	To discuss the graph algorithms, algorithms for NP Completeness Approximation Algorithms
CO4	To discuss the Graph Algorithms
CO5	To discuss the graph algorithms, algorithms for NP Hard Problems

Mapping of Course Outcomes with Program outcomes (POs)

(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1	H		M		
	CO2		M			
	CO3		H			L
	CO4	M			H	
	CO5				M	
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I INTRODUCTION 9

Polynomial and Exponential algorithms, big "oh" and small "oh" notation, exact algorithms and heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise refinement.

UNIT II DESIGN TECHNIQUES 9

Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.

UNIT III SEARCHING AND SORTING 9

Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior

UNIT IV GRAPH ALGORITHMS **9**

Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and algorithms,max-flow min cut theorem, Steiglitz's link deficit algorithm Kleitman's.

UNIT V SELECTED TOPICS **9**

NP Completeness Approximation Algorithms, NP Hard Problems, Strasseu's Matrix Multiplication Algorithms, Magic Squares, Introduction To Parallel Algorithms and Genetic Algorithms, Monte-Carlo Methods, Amortised Analysis.

TEXT BOOK:

1. E.Horowitz and S.Sahni, "Fundamentals of Computer Algorithms", Galgotia Publicatio
2. D.E.Goldberg, "Genetic Algorithms: Search Optimization and Machine Learning", Addison Wesley, 1989.

REFERENCES:

1. Sara Baase, "Computer Algorithms : Introduction to Design and Analysis", Addison Wesley,1988.
2. T.H.Cormen, C.E.Leiserson and R.L.Rivest, "Introduction to Algorithms", McGraw Hill, 1994.

Course Code	**Course Name: ROBOTICS**	**L**	**T**	**P**	**C**
MAE002	Total Contact Hours:45	3	0	0	3
	Prerequisite: Embedded systems				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES:

To study about robotic vision systems and to study robot organizations.

COURSE OUTCOMES (COs)

CO1	To develop knowledge about robot hardware.
CO2	To develop knowledge about robot control ad applications
CO3	To study basics of artificial intelligence
CO4	To study basics of Robotic vision systems
CO5	To study basics of Robot control and application

Mapping of Course Outcomes with Program outcomes (POs)

(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1			H		

	CO2	H		M		
	CO3					L
	CO4		M			
	CO5			L	M	
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT-I ROBOT ORGANIZATION
9

Coordinate transformation, kinematics and inverse kinematics, Trajectory planning and remote manipulation

UNIT-II ROBOT HARDWARE
9 Robot sensors, proximity sensors, Range sensors, visual sensors, Ausitory sensors, Robot manipulators, Manipulator dynamics , Manipulator control, acts, end efforts, Robot grippers.

UNIT III ROBOT AND ARTIFICFAL INTELLIGENCE
9 Principles of Al , Basics of learning, planning movement, Basics of knowledge presentations, Robot programming languages.

UNIT IV ROBOTIC VISION SYSTEMS
9 Principles of edge detection, Determining optical flow and shape, Image presentation, pattern recognition, Model directed scene analysis

UNIT V ROBOT CONTROL AND APPLICATION
9 Robot control using voice and infrared, overview of robot applications, prosthetic devices, Robots in material handing, processing assembly and storage.

Text Books:

1. Koren,"Robtics for Engineers", MC Graw Hill International company, Tokyo, 1995

REFERENCE BOOK:

1.Vokopravotic, "Introduction to Robotics", Springer, 1998

2. Rathmill K, "Robet Technology and Application", Springer, 1985

Course Code	Course Name: RF SYSTEM DESIGN	L	T	P	C
MAE003	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Microwave Engineering				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

The CMOS RF Front End (RFE) is a very crucial building block and in all of wireless and many high frequency wire-line systems and the RFE has few important building blocks within including the Low Noise Amplifiers, Phase Locked Loop Synthesizers, Mixers, PowerAmplifiers, and impedance matching circuits.

COURSE OUTCOMES (COs)

CO1	The student after completing this course must be able to translate the top level Wireless
CO2	Communications system specifications into block level specifications of the RFE.
CO3	The student should also able to carry out transistor level design of the entire RFE
CO4	The present course will introduce the principles of operation and design principles associated with these important blocks.
CO5	The course will also provide and highlight the appropriate digital

Mapping of Course Outcomes with Program outcomes (POs)

(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		M			
	CO2	H			H	L
	CO3			M		
	CO4		H			
	CO5		M		L	
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES

9

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct upconversion Transmitter, Two step upconversion Transmitter.

UNIT II IMPEDANCE MATCHING AND AMPLIFIERS

9

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS

9

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations , Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

UNIT IV MIXERS AND OSCILLATORS

9

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

UNIT V PLL AND FREQUENCY SYNTHESIZERS

9

Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

TEXT BOOKS:

1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge,2004.
2. B.Razavi, “RF Microelectronics”, Pearson Education, 1997.
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic.

REFERENCE BOOKS:

1. Publishers, 1997.
2. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001
3. Recorded lectures and notes available at. http://www.ee.iitm.ac.in/~ani/ee6240/

Course Code	Course Name: ADVANCED MICROPROCESSORS AND MICROCONTROLLERS	L	T	P	C
MAE005					

	Total Contact Hours:45	3	0	0	3
	Prerequisite: Microprocessors And Microcontrollers				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

- To expose the students to the fundamentals of microprocessor architecture.

COURSE OUTCOMES (COs)

CO1	The student will be able to work with suitable microprocessor / microcontroller for a specific real world application.
CO2	To introduce the advanced features in microprocessors and microcontrollers.
CO3	To enable the students to understand various microcontroller architectures
CO4	To Study the Motorola 68hc11 microcontrollers
CO5	To Study the Pic microcontroller

Mapping of Course Outcomes with Program outcomes (POs)

(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	e
2	CO1	H				
	CO2			H	M	
	CO3		H			M
	CO4			M		
	CO5		M		H	
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I MICROPROCESSOR ARCHITECTURE 9

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –

Computer principles – RISC versus CISC.

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE –PENTIUM 9

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE – ARM 9

Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

UNIT IV MOTOROLA 68HC11 MICROCONTROLLERS 9

Instruction set addressing modes – operating modes- Interrupt system- RTC-Serial Communication Interface – A/D Converter PWM and UART.

UNIT V PIC MICROCONTROLLER 9

CPU Architecture – Instruction set – interrupts- Timers- I^2C Interfacing –UART- A/D Converter –PWM and introduction to C-Compilers.

TEXT BOOK:

1. Daniel Tabak , ‘’ Advanced Microprocessors” McGraw Hill.Inc., 1995
2. James L. Antonakos , “ The Pentium Microprocessor ‘’ Pearson Education, 1997. 3. Steve Furber , ‘’ ARM System –On –Chip architecture “Addision Wesley , 2000. 4. Gene .H.Miller .” Micro Computer Engineering ,” Pearson Education , 2003.

REFERENCE BOOKS:

1. John .B.Peatman , “ Design with PIC Microcontroller , Prentice hall, 1997.
2. James L.Antonakos ,” An Introduction to the Intel family of Microprocessors ‘’ Pearson Education 1999.
3. Barry.B.Breg,” The Intel Microprocessors Architecture, Programming and Interfacing“ , PHI,2002.
4. Valvano "Embedded Microcomputer Systems" Thomson Asia PVT LTD first reprint 2001. Readings: Web links www.ocw.nit.edu www.arm.com

Course Code **MAE006**	**Course Name: HIGH SPEED SWITCHING ARCHITECTURES**	**L**	**T**	**P**	**C**
	Total Contact Hours: **45**	3	0	0	3
	Prerequisite: Computer Architectures				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES:

To enable the student to understand the basics of switching technologies and their implementation LANs, ATM networks and IP networks.

COURSE OUTCOMES (COs)

CO1	The student would be able to identify suitable switch architectures for a specified networking scenario and demonstrate its blocking performance.
CO2	The student would be in a position to apply his knowledge of switching technologies, architectures and buffering strategies for designing high speed communication networks and analyze their performance.
CO3	To enable the student to understand the different switching architectures and queuing strategies and their impact on the blocking performances.
CO4	To expose the student to the advances in packet switching architectures and IP addressing and switching solutions and approaches.
CO5	To exploit and integrate the best features of different architectures for high speed switching

Mapping of Course Outcomes with Program outcomes (POs)

(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	e
2	CO1			M		L
	CO2		H		M	
	CO3	M				
	CO4			H		M
	CO5				M	
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I LAN SWITCHING TECHNOLOGY **9**

Switching Concepts, LAN Switching, switch forwarding techniques - cut through and store and forward, Layer 3 switching, Loop Resolution, Switch Flow control, virtual LANs.

UNIT II ATM SWITCHING ARCHITECTURES **9**

Blocking networks - basic - and- enhanced banyan networks, sorting networks - merge sorting, re-arrangable networks - full-and- partial connection networks, non blocking networks -Recursive network construction, comparison of non-blocking network, Switching with deflection routing - shuffle switch, tandem banyan switch.

UNIT III QUEUES IN ATM SWITCHES **9**

Internal Queueing -Input, output and shared queueing, multiple queueing networks – combined Input, output and shared queueing - performance analysis of Queued switches.

UNIT IV PACKET SWITCHING ARCHITECTURES **9**

Architectures of Internet Switches and Routers- Bufferless and buffered Crossbar switches, Multi-stage switching, Optical Packet switching; Switching fabric on a chip; Internally buffered Crossbars.

UNIT V IP SWITCHING **9**

Addressing model, IP Switching types - flow driven and topology driven solutions, IP Over ATM address and next hop resolution, multicasting, Ipv6 over ATM.

TEXT BOOKS:

1. Achille Pattavina, "Switching Theory: Architectures and performance in Broadband ATM networks ",John Wiley & Sons Ltd, New York. 1998
2. Rich Siefert, Jim Edwards, "The All New Switch Book – The Complete Guide to LAN Switching Technology", Wiley Publishing, Inc., Second Edition, 2008.
3. Elhanany M. Hamdi, "High Performance Packet Switching architectures", Springer Publications, 2007.

REFERENCES BOOKS:

1. Christopher Y Metz, "Switching protocols & Architectures", McGraw - Hill Professional Publishing, NewYork.1998.
2. Rainer Handel, Manfred N Huber, Stefan Schroder, "ATM Networks - Concepts Protocols, Applications", 3rd Edition, Addison Wesley, New York. 1999.

Course Code	Course Name:	L	T	P	C
MDC002	**BLUE TOOTH TECHNOLOGY**				
	Total Contact Hours: 45	3	0	0	3
	Prerequisite:				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To Study Basic Concepts of Blue Tooth and to understand the structure of Bluetooth hardware, the software structure.

COURSE OUTCOMES (COs)

CO1	To develop Skill in the architecture of a Bluetooth system.
CO2	To understand the structure of Bluetooth hardware, the software structure.
CO3	To understand the functionality of a Bluetooth protocol
CO4	To Understand about Bluetooth module,Link controller and management

CO5	To Study about Bluetooth profiles and Security Issues					
Mapping of Course Outcomes with Program outcomes (POs) (H/M/L indicates strength of correlation) H-High, M-Medium, L-Low						
1	COs/Pos	A	b	c	d	E
2	CO1			H		L
	CO2	M			M	
	CO3		H			
	CO4			M		M
	CO5		H			
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT –I BASIC CONCEPTS

9 Origin, blue tooth sig, protocol stack, security, applications and profiles, management, test and qualification and technology basics, Rf and Ir wireless communication

UNIT-II BLUE TOOTH MODULE

9

Antennas patterns, gain and losses : types of antennas: on chip antennas radio interface: Fh modulation symbol timing, power emission and control , performance parameters, Rf Architecture, Blur R f, based band: blue tooth device address system timing, physical links, packet, structuring types and construction ,channel coding and time base synchronisation

UNIT-III LINK CONTROLLLER AND MANAGEMENT

9

Lep, controller states, pico net and scattered operations, master/slave role switching Lc Architectural overview, Lmc<Link set up , quality of service, Lmp version, name represent, test mode

UNIT-IV BLUETOOTH HOST

9

LIC and adaptation protocol L2cap signaling : connection; Bluetooth profiles, version 1.0 , generic profiles, serial and object exchange

UNIT-V SECURITY
9

Encryption and security key genetration, security mode and architecture, low power operation and Qos management

TEXT BOOKS:

1.Bluetooth connect without cables Jenniffer Bray and C. F. Stuntman pearson education 2001

2. Bluetooth reveeled: Brent A. Miller and C. Bisdikian, pearson education 2001

REFERENCES BOOKS:

1. Bluetooth Demystified Nathan J. Miller Tata Mc graw Hill 2001

Course Code MAE101	**Course Name: ADVANCED DIGITAL SIGNAL PROCESSING**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Digital Signal Processing				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To introduce the Concepts of silicon realization of ASIC and Cmos devices at deep Level To study and apply the deep Submicron concepts to Cmos low power devices

COURSE OUTCOMES (COs)

CO1	To learn about random signal processing
CO2	To know about spectrum and linear estimation.
CO3	To know about adaptive filters
CO4	To understand the concepts related to Adaptive Filters
CO5	To understand the concepts related to multirate digital signal processing

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2	M				
	CO3		H			
	CO4			M		
	CO5					H

3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT-1 DISCRETE RANDOM SIGNAL PROCESSING

9

Discrete Random Processes,Expectations,Variance,Co-variance,Scalar product, Energy of Discrete Signals-Parseval's Theorem, Wiener Khintchine Relation-Power Spectral Density-Periodogram-Sample Autocorrelation-Sum Decomposition Theorem, Spectral Factorization Theorem-Discrete Random Signal Processing by Linear Systems-Simulation of White Noise-Low Pass filtering of white noise.

UNIT-II SPECTRUM ESTIMATION

9

Non-Parametric Methods–Correlation Method–Co-Variance Estimator-Performance Analysis of Estimator-Barlett Spectrum Estimation –Welch Estimation-Model Based Approach-AR,MA,ARMA Signal Modeling –Parameter Estimation using Yule-Walker Method.

UNIT-III LINEAR ESTIMATION AND PREDICTION

9

Maximum likelihood criterion-efficiency of estimator-least mean squared error criterion-Wiener filter –Discrete Wiener Hoff Equation–Recursive estimators–Kalman filter–linear prediction, prediction error whitening filter, inverse filter-Levinson recursion, Lattice realization and Levinson recursion algorithm for solving Toeplitz system of equations.

UNIT-IV ADAPTIVE FILTERS

9

FIR adaptive filters-Newton's steepest descent method-adaptive filter based on steepest descent method-Widrow Hoff LMS adaptive algorithm-Adaptive channel equalization-Adaptive echocarcellor-Adaptive noise cancellation –RLS adaptive filter-Exponentially weighted RLS –Sliding window RLS –Simplified IIRLMS adaptive filter.

UNIT-V MULTIRATE DIGITAL SIGNAL PROCESSING

9

Mathematical description of sample rate-interpolation and Decimation-continuous time model direct digital approach-Decimation by an integer factor–interpolation by an integer factor-Single and multistage realization-poly phase realization-Application to Sub band coding-Wavelet transform and filter bank implementation of wavelet expansion of signals.

TEXTBOOKS:

1. Monson.H.Hayes, Statiscal Digital Processing and Modelling, John Wiley and Sons.INC, New York.1996.

REFERENCES BOOK:

1. Sophocles J.Orfanidis, OptimumSignal Processing, McGraw Hill.1990.
2. John.G.Proakis, Dimitris G.Manofakis.Digital Signal Processing Prentice Hall of India, 1995.

Course Code	Course Name: ELECTROMATIC	L	T	P	C

MAE004	**INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN**				
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Testing of VLSI Circuits				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

EMI Environment and EMI Coupling Principles and EMI Specification, Standards and Limits and EMI Measurements and Control Techniques and EMC Design of PCBs.

COURSE OUTCOMES (COs)

CO1	Ability to analyze Electromagnetic interference effects in PCBs
CO2	Ability to propose solutions for minimizing EMI in PCBs
CO3	To understand UMI Test instruments/systems,EMI Test
CO4	To understand the EMI Control Techniques
CO5	To understand the EMC Design of PCBs

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1			M		
	CO2				L	
	CO3		H			
	CO4		M			
	CO5	L				
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT-I EMI ENVIRONMENT/SPECIFICATIONS /STANDARDS

10

Sources of EMI conducted and radiated EMI, Transient EMI, EMI-EMC Definitions and units of parameters, unit of specifications, Civilian standards, and Military standards.

UNIT-II EMI COUPLING PRINCIPLES

10

Conducted, Radiated and Transient Coupling, common impedance ground coupling, radiated common mode and ground loop coupling radiated differential mode coupling, near field, cable to cable coupling, power mains and power supply coupling.

UNIT-III MEASUREMENTS **8**

UMI Test instruments/systems,EMI Test ,EMI Shielded Chamber ,Open Area Test Site ,TEM Cell Antennas ,Conductors Sensors /Injectors /Couplers ,Military Test Method AND Procedures ,Calibration procedures.

UNIT-IV EMI CONTROL TECHNIQUES **8**

Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, signal Control, Component Selection and mounting.

UNIT-V EMC DESIGN OF PCBS **9**

PCB Traces Cross Talk, Impedance Control, Power Distribution decoupling, Zoning, Motherboard Designs and propagation Delay performance models.

TEXT BOOKS:

1. Bernhard Kerser, "Principles of Electromagnetic Compatibility", Artech house, 3rd Ed 1986.
2. Henry W.Ott, "Noise Reduction Techniques in Electronic Systems", John Wiley and Sons, New York, 1986.

REFERENCE BOOKS:

1. V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, 1986.

Course Code MVL010	**Course Name: OPTIMIZATION TECHNIQUES IN VLSI DESIGN**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Basic VLSI Design				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To Know in detail about the optimization techniques and to gain knowledge on Genetic algorithms and To learn implementation of genetic algorithms for VLSI physical design problems and To understand implementation of genetic algorithms for testing of VLSI circuits and technology mapping.

COURSE OUTCOMES (COs)

CO1	To Know in detail about the Statistical Modeling
CO2	To learn implementation of genetic algorithms for VLSI physical design problems
CO3	To Know in detail about the optimization techniques
CO4	To understand implementation of genetic algorithms for testing of VLSI circuits
CO5	To understand implementation of genetic algorithms for technology mapping

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2	M				
	CO3		H			
	CO4				H	

	CO5			M		
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I STATISTICAL MODELING **9**

Modeling sources of variations, Monte Carlo techniques, Process variation modeling-Pelgrom‟s model, Principal component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models

UNIT II STATISTICAL PERFORMANCE, POWER AND YIELD ANALYSIS **9** Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation

UNIT III CONVEX OPTIMIZATION **9**

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.

UNIT IV GENETIC ALGORITHM **9**

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement,routing technology,Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multiway Partitioning Hybrid genetic-encoding-local improvement-WDFRComparison of Cas-Standard cell placement-GASP algorithm-unified algorithm.

UNIT V GA ROUTING PROCEDURES AND POWER ESTIMATION **9**

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures.Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.

TEXT BOOKS:

1. Ashish Srivastava, Dennis Sylvester, David Blaauw “Statistical Analysis and Optimization for VLSI:Timing and Power” , Springer, 2005.

2. Pinaki Mazumder, E.Mrudnick, “Genetic Algorithm for VLSI Design,Layout and test Automation”, Prentice Hall,1998

REFERENCES BOOK:

1. Stephen Boyd, Lieven Vandenberghe “Convex Optimization”, Cambridge University

Course Code MAE015	Course Name: HIGH PERFORMANCE COMMUNICATION NETWORKS	L	T	P	C
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Computer Networks				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

- To understand the basics of networks and to study packet switched networks and circuit switched networks and to study ATM ad optical networks

COURSE OUTCOMES (COs)

CO1	To develop skills in networking.
CO2	To gain knowledge in TCP/IP and ISDN concepts.
CO3	To study Internet And Tcp/Ip Networks
CO4	To study packet switched networks and circuit switched networks
CO5	To study ATM ad optical networks

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	e
2	CO1		M			
	CO2			H		
	CO3	L				
	CO4		H			L
	CO5				M	
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT-I BASIC OF NETWORKS

9 Telephone, computer, cable Television and Wireless network, Networking principles, Digitalization , service integration, network services, and layered Architecture, traffic characterization and QOS, networks services, network elements and network mechanisms

UNIT-II PACKET SWITCHED NETWORK

9 CSI and IP models: Ethernet (IEEE 802.3), tokentring(IEEE 802.5) FDDI, QDB, frame relay, SMDS, internet working with SMDS

UNIT-III INTERNET AND TCP/IP NETWORKS

9 Interview , internet protocol , TCP and VDP, performance of TCP/IP networks circuit switched networks,SONET , DWDM, Fibre to home ,DSL, Intelligent networks, CATV.

UNIT-IV ATM AND WIRELESS NETWORKS

9

Main features- addressing , signaling and routing , ATM header structure- adaptation layer, management and control, BISDN, Interworking with ATM, Wireless channel, link level design, channel access, Network design and wireless networks.

UNIT-V OPTICAL NETWORKS AND SWITCHING

9 Optical links- WDM systems, cross –connects, optical LAN'S, optical paths and networks, TDS and SDS, modular switch designs- packet switching , distributed, shared, input and output buffers

TEXT BOOKS:

1. Jean Warland and PravinVaraiya, High Performance Communication Networks, 2nd Edition , Harcourt and Morgan Kauffman , London, 2000
2. Leon Gracia, Widjaja , Communication networks, Tata McGraw Hill, New Delhi. 2000

REFERENCES BOOKS

1. SumitKasera, Pankaj sethi, ATM Networks, Tata McGraw Hill, New Delhi 2000
2. Behrouz. a. Forouzan ,Data communication and Networking , Tata McGraw Hill, New Delhi,2000

Course Code MAE014	**Course Name: INTERNET WORKING AND MULTIMEDIA**	**L**	**T**	**P**	**C**
	Total Contact Hours: **45**	3	0	0	3
	Prerequisite: Multimedia				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES:

To introduce the characteristics of text, graphics, video and speech and to teach techniques for efficient transmission of multimedia signals over networks and to introduce different network standards and parameters for quality of service.

COURSE OUTCOMES (COs)

CO1	Capability to design efficient protocols for transmission of multimedia signals over networks.
CO2	Ability to analyze the network performance
CO3	To study Multicast And Transport Protocol

CO4	To teach techniques for efficient transmission of multimedia signals over networks.
CO5	To introduce different network standards and parameters for quality of service.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	e
2	CO1		H			
	CO2	M			M	
	CO3		H			
	CO4			H		L
	CO5			M		
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I MULTIMEDIA NETWORKING 9

Digital sound, video and graphics, basic multimedia networking, multimedia characteristics, evolution of Internet services model, network requirements for audio/video transform, multimedia coding and compression for text, image, audio and video.

UNIT II BROAD BAND NETWORK TECHNOLOGY 9

Broadband services, ATM and IP , IPV6, High speed switching, resource reservation, Buffer management, traffic shaping, caching, scheduling and policing, throughput, delay and jitter performance.

UNIT III MULTICAST AND TRANSPORT PROTOCOL 9

Multicast over shared media network, multicast routing and addressing, scaping multicast and NBMA networks, Reliable transport protocols, TCP adaptation algorithm, RTP, RTCP.

UNIT IV MEDIA - ON – DEMAND 9

Storage and media servers, voice and video over IP, MPEG over ATM/IP, indexing synchronization of requests, recording and remote control.

UNIT V APPLICATIONS 9

MIME, Peer-to-peer computing, shared application, video conferencing, centralized and distributed conference control, distributed virtual reality, light weight session philosophy.

TEXT BOOKS :

1. Jon Crowcroft, Mark Handley, Ian Wakeman. Internetworking Multimedia, Harcourt Asia Pvt.Ltd. Singapore, 1998.
2. B.O. Szuprowicz, Multimedia Networking, McGraw Hill, NewYork. 1995

REFERENCES BOOK:

1. Tay Vaughan, Multimedia making it to work, 4ed,Tata McGrawHill, NewDelhi,2000.

Course Code MAE011	**Course Name: VLSI SIGNAL PROCESSING**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Digital Signal Processing				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To understand the various VLSI architectures for digital signal processing and To know the techniques of critical path and algorithmic strength reduction in the filter structures and To study the performance parameters, viz. area, speed and power.

COURSE OUTCOMES (COs)

CO1	Ability to modify the existing or new DSP architectures suitable for VLSI
CO2	To know the techniques and algorithmic strength reduction in the filter structures
CO3	To understand the various VLSI architectures for digital signal processing
CO4	To study the performance parameters area.
CO5	To study the performance parameters speed and power

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2			M		
	CO3		H			
	CO4	L				
	CO5		H			
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			

4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016

UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS 9

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm,Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION 9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 9

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TEXT BOOKS:

1. **1.** Keshab K. Parthi, "VLSI Digital Signal Processing Systems", Design and implementation, Wiley, Inter Science, 1999.
2. S.Y. Kung, H.J. White House, T.Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.

REFERENCE BOOK:

1. Jose E. France, Yannis Tsividis, "Design of Analog – Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.

Course Code	Course Name: DSP INTEGRATED CIRCUITS	L	T	P	C
MAE004	Total Contact Hours:45	3	0	0	3
	Prerequisite: Digital Signal Processing				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To familiarize the concept of DSP and DSP algorithm and Introduction to Multirate systems and finite word length effects and to know about the basic DSP processor architectures and the

synthesis of the processing elements	
COURSE OUTCOMES (COs)	
CO1	Get to know about the Digital Signal Processing concepts and it's algorithms Get an idea about finite word length effects in digital filters
CO2	Concept behind multirate systems is understood
CO3	Get familiar with the DSP processor architectures and how to perform synthesis of processing elements
CO4	Acquire an general idea about VLSI circuit layout design aspects
CO5	To gather an idea about the VLSI circuit layout design styles

Mapping of Course Outcomes with Program outcomes (POs)

(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1	H				
	CO2		M		M	
	CO3		H		H	
	CO4	H		H		L
	CO5		H			
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

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UNIT I INTRODUCTION TO DSP INTEGRATED CIRCUITS 9

Introduction to Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms, Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design.

UNIT II DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters,

Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT III DSP ARCHITECTURES 9

DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture. TMS320C54x and TMS320C6x architecture, Motorola DSP56002 architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures.

UNIT IV SYNTHESIS OF DSP ARCHITECTURES AND ARITHMETIC 9

Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

Arithmetic Unit : Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator.

UNIT V CASE STUDY-INTEGRATED CIRCUIT DESIGN 9

Layout of VLSI circuits, Layout Styles, Case Study : FFT processor, DCT processor and Interpolator.

TEXT BOOK:

1. Lars Wanhammer, "DSP Integrated Circuits", Academic press, New York, 1999.
2. John J. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Pearson Education,2002.
3. B.Venkatramani, M.Bhaskar, "Digital Signal Processors", Tata McGraw-Hill, 2002.

REFERENCE BOOK:

1. Emmanuel C. Ifeachor, Barrie W. Jervis, " Digital signal processing – A practical approach", Tata McGraw-Hill, 2002.
2. Keshab K.Parhi, "VLSI Digital Signal Processing Systems design and Implementation", John Wiley & Sons, 1999.

Course Code MVL202	**Course Name: LOW POWER VLSI DESIGN**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: VLSI Design				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To know the sources of power consumption in CMOS circuits and To understand the various power reduction techniques and the power estimation methods and

COURSE OUTCOMES (COs)

CO1	To know the basics and advanced techniques in low power
CO2	To design as reduction of power is much needed to enhance the performance of the system

CO3	To study the design concepts of High power circuits.
CO4	To understand the various power reduction techniques and the power estimation
CO5	To study the design concepts of low power circuits.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		M			
	CO2		H			L
	CO3	L				
	CO4			M		M
	CO5				L	
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I INTRODUCTION 9

Introduction – Simulation – Power Analysis – Probabilistic Power Analysis.

UNIT II ARCHITECTURE 9

Circuit – Logic – Special Techniques – Architecture and Systems.

UNIT III ADVANCED TECHNIQUES 9

Advanced Techniques – Low Power CMOS VLSI Design – Physical of Power Dissipation in CMOS FET Devices.

UNIT IV POWER ESTIMATION 9

Power Estimation – Synthesis for Low Power – Design and Test of Low Voltages – CMOS Circuits.

UNIT V LOW POWER ESTIMATION 9

Low Power Static RAM Architectuers – Low Energy Computing Using Energy Recovery Techniques – Software Design for Low Power.

Text Books:

1. **1.** Gary Yeap “Practical Low Power Digital VLSI Design”, 1997.

References:

1. Kaushik'Roy, Sharat Prasad, "Low Power VLSI Circuit Design" 2000.

Course Code MVL003	**Course Name: ANALOG VLSI DESIGN**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Basic VLSI Design				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To study the concepts of CMOS and BICMOS analog circuits and To understand the concepts of A/Dconvertors and analog integrated sensors and To understand the testing concepts in analog vlsi circuits and its statistical modelling.

COURSE OUTCOMES (COs)

CO1	To Understand that analog circuits are essential in interfacing and building amplifiers and low p filters.
CO2	To understand the concepts of A/D convertors and analog integrated sensors
CO3	To understand the concepts of CMOS and BICMOS analog circuits
CO4	To understand the testing concepts in analog vlsi circuits.
CO5	To understand the testing concepts in statistical modeling.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2		H			
	CO3	L		M		M
	CO4		M		M	
	CO5	M		M		
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT-I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW VOLTAGE SIGNAL PROCESSING 9

Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques –Super MOS Transistor-Primitive Analog Cells-Linear Voltage-Current converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low BiCMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT-II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT-MODE SIGNAL MESSING AND NEURAL INFORMATION PROCESSING

9

Continuous-Time Signal Processing-Sampled-Data Signal Processing-artiched-current Data Converters-Practical Consideration in SI Circuits Logically-Inspired Neural Networks-Floating-Gate,Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-contrast Sensitive Silicon Retina

UNIT III SAMPALED-DATA ANALOG FILTERS,OVER SAMPLED A/D CONVERTERS AND ANALOG INTERGRATED SENSORS

9

First-order and second SC Circuits-Bilinear transformation-Cascade Design-Switched-Capacitor Ladder-Synthesis of Switched –Current filter-Nyquist rate A/D converters-Modulators for over Sampled A/D conversion- First and second Order and Multibit Sigma-Delta Modulators-interpolative Modulators-Cascade Architecture-Decimation Filters-Mechanical, Thermal, Humidity and Magnetic Sensors-Sensor interfaces.

UNIT IV DESIGN FOR TESTABLITY AND ANALOG VLSI INTERCONECTORS

9

Faults modeling and Simulation- Testability-Analysis Technique-AdHoc Methods and General Guidelines Scan Techniques-Boundary Scan-Built-in self Test- Analog Test Buses-Design for Election-Beam Testability-Physics of Interconnects in VLSI- Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping analog Circuits.

UNIT V STATISTICAL MODELLING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT 9

Review of statistical concepts- statistical Device Modeling-Statistical Circuit Simulation-Automation Analog Circuit Design-Automatic Analog Layout-CMOS Transistor layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog-Digital Layout.

TEXT BOOKS:

1. ”Analog VLSI Signal and information Processing”,Mohammed Ismail,Terri Fiez, McGraw-Hill International Editions,1994.

REFERENCE BOOK:

1. Malcom R. Haskard, Lan C. May, “Analog VLSI Design- NMOS and CMOS”, Prentice hall,1998.
2. Randall I. Geiger, Phillip & Allen, Neol K. Strader, “VLSI Design Techiniques for Analog and Digital Circuits”, McGraw Hill International Company,1990
3. Jose E. France, Yannis Tsividis, “Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing,” Prentice Hall, 1994

Course Code MED102	**Course Name: EMBEDDED SYSTEMS**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3

	Prerequisite: Microprocessor and its Application
	Course Designed by : Dept. of Electronics And Communication Engineering

OBJECTIVES

To know about the concepts of embedded hardware and to know in detail about PIC microcontroller.

COURSE OUTCOMES (COs)

CO1	To understand about the basics of embedded system and its software environment
CO2	To design embedded system for real time applications.
CO3	To know in detail about embedded microcontroller.
CO4	To discuss about the software environment in embedded systems.
CO5	To learn about real time operating systems.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1			H		
	CO2				H	
	CO3		L			
	CO4			M		
	CO5				M	
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT – I INTRODUCTION REVIEW OF EMBEDDED HARDWARE 9

Terminology Gates – Timing Diagram – Memory – Microprocessors Busses – Direct Memory Access – Interrupts – Built – Ins on the Microprocessor – Conventions used on Schematic – Interrupt Microprocessor Architecture – Shared Data Problem – Interrupt Latency.

UNIT – II PIC MICROCONTROLLER AND INTERFACING 9

Introduction – CPU Architecture – Registers – Instruction Sets Addressing Modes – Loop Timers - Interrupts – Interrupt Timing I/O Expansion – 12C Bus Operation Serial EEPROM – Analog to Digital Converter – UART Baud Rate – Data Handling – Initialization – Special Features – Serial Programming – Parallel Slave Port.

UNIT – III EMBEDDED MICROCONTROLLER SYSTEMS
9

Motorola MC68H11 Family Architecture Registers - Addressing Modes – Programs – Interfacing Methods – Parallel I/O Interface – Parallel Port Interface – Memory Interfacing – High Speed I/O Interfacing - Interrupts – Interrupt SERVICE Routing – Features of Interrupts – Interrupt Vector and Priority – Timing Generation and Measurement – Input Capture – Output Compare – Frequency Measurement – Serial I/O Devices RS232, RS485 – Analog Interfacing – Applications.

UNIT – IV SOFTWARE DEVELAPMENT AND TOOLS
9

Embedded System Evolution Trends – Round – Robin with Interrupts – Function –One – Scheduling Architecture – Algorithms – Introduction to Assembler – Compiler – Cross Compilers and Integrated Development Environment (IDE) – Object Oriented Interfacing – Recursion – Debugging Strategies – Simulators.

UNIT –V REAL TIME OPERATING SYSTEMS
9

Task and Task States – Tasks and Data – Semaphores and Shared Data Operating System Services – Message Queues – Timer Function – Events – Memory Management – Interrupt Routines in an RTOS Environment – Basic Design Using RTOS.

TEXT BOOKS:

1. David E. Simon, "An embedded Software Primer" Pearson Education Asia, 2001.
2. John B Peat man "Design with Microcontroller" Pearson Education Asia, 1998.
3. Jonathan W. Volcano Brooks/Cole "Embedded Micro Computer Systems. Real Time Interfacing". Thomson Learning 2001.

REFERENCES BOOK:

1. Burns, Alan and Welling, Andy, "Real - Time Systems and Programming Languages", Second Edition, Harlow: Addison – Wesley – Longman, 1997
2. Raymond J. A. Blur and Donald L. Bailey, "Introduction to Real Time Systems: Design to Networking with C/C++" Prentice Hall Inc. New Jersey, 1999
3. Graham Moore, and Cylix, "Real – Time Programming: A Guide to 32 Bit Embedded Development. Reading" Addison - Wesley – Longman, 1998.

Course Code MED201	**Course Name: ASIC DESIGN**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Basic ASIC				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To learn the fundamentals of ASIC and its design methods

COURSE OUTCOMES (COs)

CO1	To gain knowledge about partitioning
CO2	To analyses the synthesis
CO3	To gain knowledge on programmable architectures for ASICs
CO4	To understand the physical design of ASIC.
CO5	To understand the Asics Construction, Floor Planning, Placement And Routing

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1			H		

	CO2			M		
	CO3				L	
	CO4		M			
	CO5			M		
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT – I INTRODUCTION TO ASIC, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Capacitance – Logical Effort – Library Cell Design – Library Architecture Types of ASIC **–** Design Flow – CMOS Transistors – CMOS Design Rules – Combinational Logic Cell – Sequential Logic Cell – Data Path Logic Cell – Transistors as Resistors – Transistor Parasitic**.**

UNIT –II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS. 9

Ant fuse – Static RAM – EPROM and EEPROM Technology – PREP Bench Marks – Acted ACT – Xilinx LCA – Altars FLEX – Alters MAX – DC & AC Input and Output – Clock and Power Input – Xilinx I/O Blocks.

UNIT – III PROGRAMMABLE ASICS INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY.

9

Acted ACT - Xilinx LCA - Xilinx EPLD - Alters MAX 5000 & 7000 - Alters MAX 9000 - Alters FLEX – Design System – Logic Synthesis – Half Gate ASIC – Schematic Entry – Low Level Design Language – PLA Tools – EDIF – CFI Design Representation**.**

UNIT – IV LOGIC SYNTHESIS, SIMULATION AND TESTING

9

Verilog and Logic Synthesis– VHDL and LOGIC Synthesis– Types of Simulation – Boundary Scan Test– Fault Simulation- Automatic Test Pattern Generation.

UNIT – V ASICS CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING.

9

System Partition – FPGA Partitioning – Partitioning Methods – Floor Planning – Placement – Physical Design Flow – Global Routing – Detailed Routing – Special Routing –Circuit Extraction – DRC.

TEXT BOOK:

1. M. J. S. Smith, “Application Specific Integrated Circuits” , Addison – Wesley L Ongnam Inc., 1997.

REFERENCE BOOK:

1. Andrew Brown, “VLSI Circuits and Systems in Silicon”, McGraw Hill 1991.
2. S. D. Brown, R. J. Francis, J. ROX, Z. G. Urines, “Field Programmable Publishers, 1992.
3. Mohammed Ismail and Terri Fief, “Analog VLSI and Modern Signal Processing,” McGraw Hill 1994.
4. S. Y. Kang, H. J. While Hours, T. Kailath, “VLSI Modern Signal Processing,” Prentice Hall, 1985. Jose E. France, Yantis Tsividis, “Design of Analog – Digital VLSI Circuits for Telecommunication and Signal Processing”, Prentice Hall, 1994.