CURRICULUM AND SYLLABUS (R2015)

CHOICE BASED CREDIT SYSTEM

M.TECH-EMBEDDED SYSTEM DESIGN
(FULL TIME)
I – IV SEMESTERS

SEMESTER-I					
Sub Code	**Subject Name**	**L**	**T**	**P**	**C**
Theory					
MMA101	Applied Mathematics for Electronics Engineers	3	1	0	4
MES101	Microcontroller Based System Design	3	0	0	3
MES102	Embedded Systems	3	0	0	3
MAE102	Advanced Digital System Design	3	0	0	3
MES1E1	Elective-I	3	0	0	3
Practical					
MES1L1	Embedded System Design Lab-I	0	0	4	2
				Total Credits:	**18**

SEMESTER-II					
Sub Code	**Subject Name**	**L**	**T**	**P**	**C**
Theory					
MES201	ASIC Design	3	0	0	3
MES202	Software Technology for Embedded System	3	0	0	3
MES203	Real Time Systems	3	0	0	3
MES2E2	Elective-II	3	0	0	3
MES2E3	Elective-III	3	0	0	3
Practical					
MES2L2	Embedded System Design Lab-II	0	0	4	2
				Total Credits:	**17**

SEMESTER-III					
Sub Code	**Subject Name**	**L**	**T**	**P**	**C**
Theory					
MES3E4	Elective-IV	3	0	0	3
MES3E5	Elective-V	3	0	0	3
MES3E6	Elective-VI	3	0	0	3
MES3P1	Project work phase-I	0	0	12	6
				Total Credits:	**15**

SEMESTER-IV					
Sub Code	**Subject Name**	**L**	**T**	**P**	**C**
MES4P2	Project work phase-II	0	0	24	12
				Total Credits:	12

TOTAL CREDITS FOR THE PROGRAMME-62

Sub Code	LIST OF ELECTIVES	L	T	P	C
MED 001	Design of Embedded System	3	0	0	3
MED 002	Embedded Control System	3	0	0	3
MED 003	Computer Vision and Image Understanding	3	0	0	3
MED 004	Distributed Embedded Computing	3	0	0	3
MED 005	Design of Digital Control System	3	0	0	3
MED 006	Crypto Analytic Systems	3	0	0	3
MED 007	Intelligent Embedded Systems	3	0	0	3
MED 008	Real Time Operating System	3	0	0	3
MED009	Advanced Microprocessors	3	0	0	3
MED010	Artificial Intelligence and Expert systems	3	0	0	3
MED011	Advanced Digital Signal Processing	3	0	0	3
MED012	Computer Architecture and parallel processing	3	0	0	3
MED013	Design of semiconductor Memories	3	0	0	3
MED014	VLSI Architecture and Design methodologies	3	0	0	3
MED015	Introduction to VLSI Design	3	0	0	3
MST070	Research Methodology	3	0	0	3

SEMESTER-I

MMA101 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS 3 1 0 4

Course Objective:

- To apply all taught techniques to unseen problems,
- Queuing is a major branch of optimization, Random variable compute and interprets means.
- Correlation/covariance, PERT and CPM chart is mainly used for documenting the data(visually) on projects.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: The Student will learn to analyze and solve the fundamental problems with prescribed conditions in simple cases.

CO2: The Student will learn to understand how signals, systems, inference combine in prototypical tasks of communication, control and signal processing.

CO3: The Student will learn to manipulate matrices and to do Matrix algebra, determinants, Eigen values Eigen vectors and to solve the system of linear equations.

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S		M									
CO2		M		W	S	W						
CO3			S		M							
CO4	M			M								
CO5												

UNIT-I: ONE DIMENSIONAL RANDOM VARIABLES 12

Random variables and their functions - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Exponential, Gamma, Weibull and Normal distributions.

UNIT-II: MATRIX THEORY 12

Eigen values using QR Transformations generalized eigenvectors – Canonical forms, singular valued composition and application – matrix norms and induced norms Psuedo inverse – least square approximations.

UNIT-III: SPECIAL FUNCTIONS 12

Bessel's Equation- Bessel Functions- Legendre's Equation- Legendre Polynomials- Rodrigue's Formula- Recurrence Relations- Generating Functions and Orthogonal Property for Bessel Function of the First Kind.

UNIT- IV: OPERATIONS RESEARCH **12**

Network Definitions – Minimal Spanning Tree algorithm – Shortest Route Problem – Maximal Flow model – Minimum Cost Capacitated Flow Problem – CPM and PERT**.**

UNIT-V : QUEUEING THEORY **12**

Single and Multiple Server Markovain Queuing Models – Customer Impatience Priority Queues M/g / I Queuing System –Queuing Applications

. **Total Periods: 60 Hours**

Reference Books:

1. Freund J.D. and Miller JR "Probability Statistics for Engineers" Prentice Hall of India, 5th Edition, New Delhi. 1994.
2. Gupta.SC and Kapoor V.K. "Fundamentals of Mathematics Statistics" Sultan Chand & Sons, New Delhi.
3. Steart G.W. "Introduction to Matrix Computaions" Academic Press, New York.
4. Handy A.Taha., "Operations Research An Introduction", 7th Edn. Pearson Education , Chennai-113. 2002.
5. Donald Gross and Carl M. Harris, "Fundamentals of Queuing Theory", 2nd Edn. Wiley India Pvt Ltd, New Delhi.

MES101 MICROCONTROLLER BASED SYSTEM DESIGN 3 0 0 3

Course Objectives:

- To teach I/O and RTOS role on microcontroller.
- To impart knowledge on PIC Microcontroller based system design.
- To introduce Microchip PIC 8 bit peripheral system Design
- To give case study experiences for microcontroller based applications.

Course Outcomes

After successful completion of this course, the students should be able to

CO1: review 8-bit microcontrollers

CO2: learn assembly and C-programming of PIC

CO3: learn Interfacing of Microcontroller

CO4: get familiar with real time operating system

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12

CO1	S	M		M	W		S	M				
CO2	M		M	M	S		M		M			
CO3	S	M		S	M		S	M				
CO4	S	M		M	M							

UNIT-I **9**

INTEL8051

Architecture of 8051 - memory organization - register banks - register banks - bit addressable area - SFR area - addressing modes - instruction set - programming examples.

UNIT-II **9**

8051 interrupt structure – timer modules – serial features – port structure – power saving modes – family features; 8031/8071.

UNIT-III **9**

MOTOROLA 68HC11;

68HC11 features – different modes of operation and memory map – functions of I/O ports in single chip and expanded multiplexed mode-timer system of 68HC11.

UNIT-IV **9**

Input capture, output compare and pulsed accumulator features of 68hc11-serial peripheral and serial communication interface – analog to digital conversion features- - watchdog features.

UNIT-V **9**

8096 CONTROLLER

Architecture of 8096 – modes – block diagram of interrupt structure – timers – high speed input and outputs – PWM output – analog interface – serial ports.

TYPICAL APPLICATION:

Stepper motor control – dc motor control – AC power control – introduction to microcontroller development tools.

Total Periods: 45 Hours

Reference Books:

1. The 8051 Microcontroller Based Embedded Systems Paperback – 14 May 2014by Manish K Patel.
2. ”8 – bit embedded controllers”, INTEL corporation 1990.
3. ” 16 – bit embedded controllers hand book”, INTEL corporation 1989.
4. JOHN B Peatman,”desigh with Microcontroller”,Mc Grew Hill, Singapore

MES102 EMBEDDED SYSTEMS 3 0 0 3

Course Objectives:

- To know about the concepts of embedded hardware.
- To know in detail about PIC microcontroller.
- To know in detail about embedded microcontroller.
- To discuss about the software environment in embedded systems.
- To learn about real time operating systems.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: To understand about the basics of embedded system and its software environment

CO2: To design embedded system for real time applications.

CO3: Describe the differences between the general computing system and the embedded system, also recognize the classification of embedded systems.

CO4: Become aware of the architecture of the ATOM processor and its programming aspects (assembly Level)

CO5: Become aware of interrupts, hyper threading and software optimization.

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S		M									
CO2		M		W	S	M	S	M				
CO3			S		M							
CO4	M			M			M					
CO5												

UNIT – I

INTRODUCTION REVIEW OF EMBEDDED HARDWARE 9

Terminology Gates – Timing Diagram – Memory – Microprocessors Busses – Direct Memory Access – Interrupts – Built – on the Microprocessor – Conventions used on Schematic – Schematic. Interrupt Microprocessor Architecture – Shared Data Problem – Interrupt Latency.

UNIT – II

UNIT PIC MICROCONTROLLER AND INTERFACING 9

Introduction – CPU Architecture – Registers – Instruction Sets Addressing Modes – Loop Timers - Interrupts – Interrupt Timing I/O Expansion – 12C Bus Operation Serial EEPROM – Analog to Digital Converter – UART Baud Rate – Data Handling – Initialization – Special Features – Serial Programming – Parallel Slave Port.

UNIT – III

EMBEDDED MICROCONTROLLERSYSTEMS 9

Motorola MC68H11 Family Architecture Registers - Addressing Modes – Programs – Interfacing Methods – Parallel I/O Interface – Parallel Port Interface – Memory Interfacing – High Speed I/O Interfacing - Interrupts – Interrupt Service Routing – Features of Interrupts – Interrupt Vector and Priority – Timing Generation and Measurement – Input Capture – Output Compare – Frequency Measurement – Serial I/O Devices RS232, RS485 – Analog Interfacing – Applications.

UNIT – IV

SOFTWARE DEVELAPMENT AND TOOLS 9

Embedded System Evolution Trends – Round – Robin with Interrupts – Function –One – Scheduling Architecture – Algorithms – Introduction to Assembler – Compiler – Cross Compilers and Integrated Development Environment (IDE) – Object Oriented Interfacing – Recursion – Debugging Strategies – Simulators.

UNIT –V

REAL TIME OPERATING SYSTEMS 9

Task and Task States – Tasks and Data – Semaphores and Shared Data Operating System Services – Message Queues – Timer Function – Events – Memory Management – Interrupt Routines in an RTOS Environment – Basic Design Using RTOS.

Total Periods: 45 Hours

Text books:

1. Embedded Systems: Introduction to Arm(r) Cortex -M Microcontrollers: 1Paperback – Import, 26 May 2012by Jonathan W Valvano (Author)
2. David E. Simon, "An embedded Software Primer" Pearson Education Asia, 2001.
3. John B Peat man "Design with Microcontroller" Pearson Education Asia, 1998.
4. Jonathan W. Volcano Brooks/Cole "Embedded Micro Computer Systems. Real Time Interfacing". Thomson Learning 2001.
5. Embedded systems: architecture, programming and design paperback – 11 Jun 2008by Raj Kamal (Author)

Reference Books:

1. Burns, Alan and Welling, Andy, "Real - Time Systems and Programming Languages", Second Edition, Harlow: Addison – Wesley – Longman, 1997
2. Raymond J. A. Blur and Donald L. Bailey, "Introduction to Real Time Systems: Design to Networking with C/C++" Prentice Hall Inc. New Jersey, 1999
3. Graham Moore, and Cylix, "Real – Time Programming: A Guide to 32 Bit Embedded Development. Reading" Addison - Wesley – Longman, 1998.
4. Heath. Steve, "Embedded Systems Design", Newness1997.

MAE102 ADVANCED DIGITAL SYSTEM DESIGN 3 0 0 3

Course objectives:

- To learn the concepts of theorems and other techniques to design minimized logic functions.
- To Understand the concepts of synchronous and asynchronous sequential circuit design
- To learn about the faults in logic circuits and methods of diagnosing it.
- To learn about programmable logic devices.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: The candidate should after this course have an in-depth knowledge of digital integrated circuit hardware design.

CO2: The emphasis is on FPGA technology, but most of the design techniques can also be applied to ASIC devices.

CO3: The student should be familiar with the latest state-of-the-art system on chip (SoC) design methodologies, including high-level synthesis and partial run-time reconfiguration.

CO4: Students should be able to learn the benefits and drawbacks of the various design methods for solving a problem.

CO5: Through practical assignments, experience will be achieved from both using tools as well as designing their own system.

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1							S					
CO2		S	S	M	M				S	M		
CO3	S					M			M			
CO4		M	S	W		S			S	M		
CO5	S				M							

UNIT-1

ADVANCED TOPICS IN BOOLEAN ALGEBRA 9

Shannon's expansion theorem, Consensus theorem, Octal designation, Run measure, INHIBIT/INCLUSION/AOI/Driver /Buffer gates ,Gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method ,Design of static hazard free and dynamic hazard free logic circuits.

UNIT-II

THRESHOLD LOGIC 9

Linear seperability, Unateness, Physical implementation, Dual comparability, reduced function, various theorems in threshold logic, Synthesis of single gate and multigate threshold Network

UNIT-III

SYMMETRIC FUNCTIONS **9**

Elementary symmetric functions, partially symmetric and totally symmetric functions, McCluskey decomposition method, Unity ratio symmetric ratio functions, Symmetric ratio functions, Synthesis function by contact networks.

UNIT-IV

SEQUENTIAL LOGIC CIRCUITS **9**

Mealy machine, Moore Machine, Trivial/ Reversible /Isomorphic sequential machines, state diagrams, State table minimization incompletely specified sequential machines ,State assignments ,Design of synchronous and asynchronous sequential logic circuits working in the fundamental mode and pulse mode, Essential Hazards.

UNIT-V

PROGRAMMMABLE LOGIC DEVICES **9**

Basic concepts, Programming technologies, Programmable Logic Element(PLE),Programmable Logic Array(PLA),System Design using PLD's-Design of combinational and sequential circuits using PLD's(CPLD).Programming PAL device using PALSAM ,Design of state machine using Algorithmic State Machines (ASM) chart as a design tool, Introduction to Field Programmable Gate Arrays –Types of FPGA, Xilinx XC 3000 series, Logic Cell Array (LCA),Configurable Logic Blocks(CLB) INPUT/OUTPUT Block(IPB)-Programmable Interconnect Point (PIP),Introduction to Actel AACT2 FAMILY AND XILINX XC 4000 families ,Design examples.

Total Periods: 45 Hours

Reference Books:

1. William I.Flectcher, "An Engineering Approach to Digital Design", PrenticeHall of India.
2. James E.Palmer, David E.Perlman, "Introduction to Digital Systems", Tata McGraw Hill, 1996.
3. N.N.Biswas, "Logic Design Theory ", Prentice Hall of India, 1993
4. S.Devadas, A.Ghosh and K.Keutzer, "Logic Synthesis", McGraw Hill, 1994.

MES1L1 EMBEDDED SYSTEM DESIGN LAB-1 0 0 4 2

(EXPERIMENTS SHOULD BE DONE USING PIC/8051 MICROCONTROLLER)

Course objectives:

- Understand the problem to be solved by incorporating PIC microcontroller.
- Identify the appropriate interfacing device for the problem.
- Design and execution of interfacing circuits.
- Practice simple programming in PIC.
- Experiment with peripheral devices on the PIC evaluation kit.

Course outcomes:

After successful completion of this course, the students should be able to

CO1: Students will learn about the interfacing concepts and implement it by using PIC microcontroller.

CO2: Practice simple programming in ARM.

CO3: Employ and test thumb and special instructions ARM in programs.

CO4: Develop algorithms and code for I/O with ARM.

CO5: Experiment with peripheral devices on the ARM evaluation kit

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
Cos	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S	S		S			S	M		S	
CO2	S	M			S			S	M		S	
CO3	M		M		S			S	M		S	
CO4	S	M			S			S	M		S	
CO5	S	M			S			S	M		S	

LIST OF EXPERIMENTS

1. ADC Interface Experiment with Temperature Sensor.
2. Stepper Motor Interface.
3. Traffic Light Controller.
4. Dac/Dc Motor Speed Control.
5. PIC To PC Serial (Rs232) Communication.
6. 5 X 7 Matrix Led Display Interface And 16 X 2 Character Lcd Interface.
7. 4x4 Hex Board Interface.
8. Programmable Logic Control

MES201 ASIC DESIGN 3 0 0 3

Course objectives:

- To learn the fundamentals of ASIC and its design methods
- To gain knowledge on programmable architectures for ASICs
- To understand the physical design of ASIC.

Course Outcomes

After successful completion of this course, the students should be able to

CO1: To gain knowledge about partitioning, floor planning, placement and routing including circuit extraction of ASIC.

CO2: To analyse the synthesis, Simulation and testing of systems.

CO3: Describe the different phases of the design flow for digital ASICs.
CO4: Explain how non-functional design constraints affect the design process.
CO5: Categorize different types of ASICs and explain their technology.

CO/PO Mapping
(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1			S	M								
CO2	S	M	M		S	S			S	M		
CO3				S	W			S	M		M	
CO4		S	W		M	W	S		S	M		
CO5	M								S	M		

UNIT – I **9**

INTRODUCTION TO ASIC, CMOS LOGIC AND ASIC LIBRARY DESIGN

Capacitance – Logical Effort – Library Cell Design – Library Architecture Types of ASIC – Design Flow – CMOS Transistors – CMOS Design Rules – Combinational Logic Cell – Sequential Logic Cell – Data Path Logic Cell – Transistors as Resistors – Transistor Parasitic.

UNIT – II **9**

PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS.

Ant fuse – Static RAM – EPROM and EEPROM Technology – PREP Bench Marks – Acted ACT – Xilinx LCA – Altars FLEX – Alters MAX – DC & AC Input and Output – Clock and Power Input – Xilinx I/O Blocks.

UNIT – III **9**

PROGRAMMABLE ASICS INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY.

Acted ACT - Xilinx LCA - Xilinx EPLD - Alters MAX 5000 & 7000 - Alters MAX 9000 - Alters FLEX – Design System – Logic Synthesis – Half Gate ASIC – Schematic Entry – Low Level Design Language – PLA Tools – EDIF – CFI Design Representation.

UNIT – IV

LOGIC SYNTHESIS, SIMULATION AND TESTING **9**

Verilog and Logic Synthesis– VHDL and LOGIC Synthesis– Types of Simulation – Boundary Scan Test– Fault Simulation- Automatic Test Pattern Generation.

UNIT – V **9**

ASICS CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING.

System Partition – FPGA Partitioning – Partitioning Methods – Floor Planning – Placement – Physical Design Flow – Global Routing – Detailed Routing – Special Routing –Circuit Extraction – DRC.

Total Periods: 45 Hours

Text Books:

1. M. J. S. Smith, "Application Specific Integrated Circuits" , Addison – Wesley L Ongnam Inc., 1997.
2. A Guide to Modern ASIC Design: From Register Transfer Level to Logic Synthesis Hardcover – Import, 1 Jun 2010by Victor X. Q. Yu (Author), Albert T. L. Lee (Author), Philip C. H. Chan (Author)

Reference Books:

1. Andrew Brown, "VLSI Circuits and Systems in Silicon", McGraw Hill 1991.
2. S. D. Brown, R. J. Francis, J. ROX, Z. G. Urines, "Field Programmable Publishers, 1992.
3. Mohammed Ismail and Terri Fief, "Analog VLSI and Modern Signal Processing," McGraw Hill 1994.
4. S. Y. Kang, H. J. While Hours, T. Kailath, "VLSI Modern Signal Processing," Prentice Hall, 1985.
5. Jose E. France, Yantis Tsividis, "Design of Analog – Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.

MED202 SOFTWARE TECHNOLOGY FOR EMBEDDED SYSTEMS 3 0 0 3

Course Objectives

- To demonstrate professional advancement through significant technical achievements and expanded leadership responsibility;
- Demonstrate the ability to work effectively as a team member and/or leader in an ever-changing professional environment; and
- Progress through advanced degree or certificate programs in computing, science, engineering, business, and other professionally related fields.

Course Outcomes

After successful completion of this course, the students should be able to

CO1: Identify and understand the working of key components of a computer system (hardware, software, firmware etc).

CO2: Understand computing environment, how computers work and the strengths and limitations of computers.

CO3: Identify and understand the various kinds of input-output devices and different types of storage media commonly associated with a computer.

CO4: Identify and understand the representation of numbers, alphabets and other characters in computer system.

CO5: Understand, analyze and implement software development tools like algorithm, pseudo codes and programming structure.

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1			S	M				S	M			
CO2	S	M	M		S	S		M		M		
CO3				S	W			S	M			
CO4		S	W		M	W	S	S	M			
CO5	M											

UNIT-I **9**

LOWERLEVEL PROGRAMMING IN C

Primitive data types – functions – recursive functions – pointers – structures – unions – dynamic memory allocations – pipe handling – linked lists.

UNIT –II **9**

C AND ASSEMBLY

Programming in assembly – register usage conversions – typical use of addressing options – instruction sequencing – procedure call and return – parameter passing – retrieving parameters – everything in pass by value – temporary values.

UNIT-III **9**

OBJECT- ORIENTED ANALYSIS AND DESIGN

Connecting the object model with the use case model – key strategies for objects identification – underline the noun strategy – identify the casual objects – identity services (passive contributors)- identity real – world items – identity physical devices – identity key concepts – identity transactions – identity persistent information – identity visual elements – identity control elements – apply scenarios.

UNIT-IV

UNIFIED MODELING LANGUAGE **9**

Object state behavior – UML state charts – role of scenarios in the definition of behavior – timing diagrams – sequence diagrams - event hierarchies – types and strategies of operations – architectural design in UML concurrent design – representing tasks – system task diagram – concurrent state diagrams – threads – mechanistic design – design simple patterns.

UNIT-V

CASE STUDIES **9**

Multi threaded applications – assembling embedded applications – polled waiting loop and interrupt driven I/O – preemptive kernels and shared resources – system timer – scheduling – client server computing.

Total Periods: 45 Hours

Reference Books:

1. Bruce Powel Douglas, "real – time UML", 2nd edition :developing efficient objects for embedded systems (the Addison- Wesley object technology series)'',2nd edition (October 29, 1999), ADDISON – Wesley.
2. Hassan gomma, ''design concurrent, distributed and real – time applications with UML.
3. Daniel W.lewis,''fundamentals of embedded software where cand assembly meet '' PHI 2002.

MES203 REAL TIME SYSTEMS 3 0 0 3

Course Objectives

- To expose the students to the fundamentals of Real Time systems
- To teach the fundamentals of Scheduling and features of programming languages
- To study the data management system for real time
- To introduce the fundamentals of real time communication
- To teach the different algorithms and techniques used for real time systems

Course Outcomes

After successful completion of this course, the students should be able to

CO1: explain and apply the fundamental concepts and terminology of real-time systems;

CO2: explain and address the fundamental problems of real-time systems;

CO3: analyze real-time systems designs;

CO4: design a real-time system (at least partially); and

CO5: identify and assess the relevant literature and research trends of real-time systems.

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1			S	M					M		S	
CO2	S	M	M		S	S				S	W	
CO3				S	W			S	W		M	
CO4		S	W		M	W	S		M		S	
CO5	M											

UNIT-I

INTRODUCTION: 9

Introduction – issues in real time computing – structure of a real time system – task glasses – performances measures for real time systems – estimating program run time – task assignment and scheduling – classical uniprocessor scheduling algorithms – uniprocessor scheduling of IRIS tasks – tasks assignment – mode changes – fault tolerant scheduling.

UNIT-II

PROGRAMMING LANGUAGES AND TOOLS: 9

Language features – desired language characteristics – data typing – control structure – facilitating hierarchical decomposition – package – run – lime error handling – overloading and generics – multi tasking – low-level programming – task scheduling – lining specifications – programming environment – run-time support – code generation.

UNIT-III

REAL TIME DATA BASES 9

Real time data base- basic definition – real lime vs general – purpose database – main memory data bases – transaction priorities – transaction aborts – concurrent control issues –disk scheduling algorithms – two-phase approach to improve predictability – maintaining serialization consistency- databases for hard real time systems.

UNIT-IV

COMMUNICATION 9

Real time communication – communications media – network topologies – protocols – buffering data – synchronization – deadlock – mailboxes and semaphores – fault tolerance techniques – fault types – fault detection – fault error containment – redundancy – data diversity – reversal checks – integrated handling.

UNIT-V

EVALUATIION TECHNIQUES: 9

Reliability evaluation techniques – reliability models for hardware redundancy – software error models – response time calculations – interrupt latency – time loading and its measurement – reducing response times – latency – time loading and its measurement – reducing response times – analysis of memory requirements – reducing memory loading.

Total Periods: 45 Hours

Textbooks

1. C.M Krishna, kangG.shin, real- time systems, McGraw-hill international editions, 1997.

References

1. Straut Bennett, real time computer control – an introduction, PHI, 1998.
2. Peter D Lawrence, real time micro computer system design – an introduction, McGraw hill, 1998.
3. S.T allworth and R.N Zobel, introduction to real time software design macmillan, 2nd edition, 1987.

MES2L2 EMBEDDE SYSTEM DESIGN LAB LAB-II 0 0 4 2

Objectives:

- To learn about the design of digital circuits using Hardware description languages

- To learn about the design of FPGA based design methodology.
- To study about the design of simulation of analog building blocks.
- To understand about digital CAD design flow.
- To know about SPICE simulation.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: Design and test digital logic circuits on FPGA.

CO2: Design Electronic circuits using SPICE and PCB layout using EDA tools

CO3: To design and Test of multiplexers and coders

CO4: To design and Test of flipflops

CO5: To design and Test of counters and registers

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	P11	P12
CO1	S	S	S		S			S	M		S	S
CO2	M		S		S			S	M		S	S
CO3		S	W					S	M		S	S
CO4	W		M					S	M		S	S
CO5	M		S		S			S	M		S	S

List of Experiments

A. Vx WORKS – RTOS LAB

1. Thread Management.
2. Pipes, Message Queue & Semaphoke.
3. Ram Disk And File System.
4. Memory Management & Watching Timer.

B. VHDL LAB

1. Design of Basic Gates, Address & Subtacxters.
2. Design of Mux, Demux, Encoder, Decoder & Synchronous Counter.
3. Design of Parallel Adder, Comparator, Flip- Flops, Shift Register & Ram
4. Design of A/D Converter Using FGFA Kit

ELECTIVES

MES001 DESIGN OF EMBEDDED SYSTEMS 3 0 0 4

Course Objectives

- To provide a clear understanding on the basic concepts, Building Blocks for
- Embedded System
- To teach the fundamentals of System design with Partioning

- To introduce on Embedded Process development Environment
- To study on Basic tool features for target configuration
- To introduce different EDLC Phases &Testing of embedded system

Course Outcomes

After successful completion of this course, the students should be able to

CO1: Compare embedded system design models using different processor technologies (single-purpose, general-purpose, application specific processors).

CO2: Describe and compare the various types of peripherals used in embedded systems.

CO3: Analyze a given embedded system design and identify its performance critical points.

CO4: Use modern engineering tools necessary for integrating software and hardware components in embedded system designs.

CO5: Utilize a top-down modular design process to complete a medium complexity embedded system design project under instructor specified design constraints.

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1			S	M		M		S				
CO2	S	M	M		S		S	W				
CO3				S	W	W		M				
CO4		S	W		M	M		S				
CO5	M											

UNIT–I

INDRODUCTION **9**

Embedded computing – characteristics of embedded computing applications- embedded system design challenges – constraint driven design – IP – based – hardware – software co –design

UNIT – II

DEVELOPMENT ENVIRONMENT **9**

The Execution Environment- memory organization – system space – code space – Data space – unpopulated memory space –i/o space – system start – up – interrupt Response cycle – Function calls and stack frames- run time environment- object placement

UNIT-III **9**

EMBEDDED COMPUTING PLATFORM

CPU bus – memory devices –I/O devices –component interfacing- designing with microprocessors- development and debugging- design example –design patterns – dataflow graphs –assembly and linking – basic compilation techniques –analysis and optimization

UNIT-IV **9**

DISTRIBUTED EMBEDDED SYSTEM DESIGN

Inter –process communication –signals – signals in UML- shared memory communication- accelerated design- design for video accelerator- networks for embedded systems –networks based design- internet enabled systems

UNIT-V **9**

DESIGN TECHNIQUES

Design methodologies and tools – design flows – designing hardware and software components – requirements analysis and architecture design – system integration –structural and behavioral description – case studies

Total Periods: 45 Hours

References:

1. Morgon Kaufman Publishers
2. Jean J. Labrosse, ‘’Embedded system Building blocks ; complete and ready to use modules in C’’

MES002 EMBEDDED CONTROL SYSTEMS 3 0 0 3

Course Objectives

- To expose the students to the fundamentals of Embedded System Blocks
- To teach the fundamental RTOS.
- To study on interfacing for processor communication
- To compare types and Functionalities in commercial software tools
- To discuss the Applications development using interfacing

Course Outcomes

After successful completion of this course, the students should be able to

CO1: Explain various embedded system applications and design requirements

CO2: Construct embedded system hardware

CO3: Develop software programs to control embedded system

CO4: Generate product specification for embedded system

CO5: Outline validation and testing methodologies for embedded system

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1			S	M	M		S	M				
CO2	S	M	M			S	W					
CO3				S	W		M	W				
CO4		S	W		M		S	M				
CO5	M											

UNIT-I INTERODUCTION 9

Controlling the hardware with software – data lines number systems address lines schematic representation hit masking programmable peripheral interlace Switch input detection.

UNIT-II INPUT OUTPUT DEVICES 9

Keyboard basic – keyboard scanning algorithm – multiplexed LED displays – character LCD modules- LCD module display – configuration – time – of- day – clock – timer manager interrupts – interrupt service routines – IRQ-ISR-interrupt vector or dispatch table multiple point – interrupt – driven pulse width modulation.

UNIT-III D/A AND CONVERSION 9

R-2R ladder – more on op – amps – virtual ground – resister network analysis – port offsets – triangle waves analog Vs digital values –ADC0809- comparator – successive approximation – the ADC clock – ripple counter – D flip flop –Q and NOTQ- capturing analog information in the timer interrupt service routine – automatic, multiple channel analog to digital data acquisition.

UNIT-IV ASYNCHRONOUS SERIAL COMMUNICATION 9

Asynchronous serial communication – RS – 232 -RS – 485 – sending and receiving data _ serial ports on PC –low level PC serial I/O module – buffered serial I/O.

UNIT-V CASE STUDIES 9

Multiple closure problems – basic outputs with PPI – controlling motors – bidirectional control of motors – H bridge – telephonic systems – burglar alarms – fire alarms – inventory control systems.

Total Periods: 45 Hours

References Books:

1. Jean J. Labrosse,'' Embedded Systems Building Blocks: Complete and Ready_to_Use Moduyles in C,''the Publisher, Paultemme, 1999,
2. Ball S.R, "Embedded Microprocessor Systems_Real World Design", Prentice Hall,1996.
3. HermaK,"Real Time Systems_Design For Distributed Embedded Applications '' Kulwer Academic , 1997.
4. Daniel W.Lewis," Fundamental Of Embedded Software Where C And Assembly Meet'' PHI 2002.

MES003 COMPUTER VISION AND IMAGE UNDERSTANDING 3 0 0 3

Course Objectives

- To introduce students with practice and theory of computer vision
- To give basics of pattern recognition concepts with applications to computer vision
- To provide students with necessary theory and skills for automatic analysis of digital images, and thereby to construct representations of physical objects and scenes, and to make useful decisions based on them

Course Outcomes

After successful completion of this course, the students should be able to

CO1: Understand image formation and the role human visual system plays in perception of gray and color image data.

CO2: Get broad exposure to and understanding of various applications of image processing in industry, medicine, and defense applications

CO3: Learn the signal processing algorithms and techniques in image enhancement and image restoration.

CO4: Acquire an appreciation for the image processing issues and techniques and be able to apply these techniques to real world problems.

CO5: Be able to conduct independent study and analysis of image processing problems and techniques.

	CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak											
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S		M		W			M	S		M	
CO2	S	M		S	M	S					M	
CO3	S		S	W						M		
CO4		W		M								
CO5		M		S								

UNIT-I DIGITAL IMAGE FUNDAMENTALS **9**

Histogram transforms - walshhadamard transform- discrete cosine – hotelling transform – image formation and file formats

UNIT-II IMAGE ENHANCEMENT **9**

Histogram modification techniques – image smoothening – image sharpening – image restoration – degradation model – diagonalisation of circuit and block circulant matrices – algebraic approach to restoration

UNIT-III IMAGE COMPRESSION AND SEGMENTATION **9**

Compression models – element of information theory – error free compression – image segmentation – detection of discontinuities – edge linking and boundary detection – threshold – regions oriented segmentation - morphology

UNIT-IV FEATURE EXTRACTION **9**

Image feature description – interpretation of line drawings – image pattern – recognition algorithms

UNIT-IV KNOWLEDGE REPRESENTATION AND USAGE **9**

Knowledge representation and usage – image analysis knowledge about scenes – image understanding using two dimensional methods.

Total Periods: 45 Hours

References

1. GONZALEZ .R & woods B.E "Digital Image Processing", Addision Wesley, 1993
2. ANIL Jain .K "Fundamental Digital Image Processing" Prentice Hall Of India 1983

MES004 DISTIBUTED EMBEDDED COMPUTING 3 0 0 0

Course Objectives

- To understand the hardware infrastructure of distributed systems.
- To study concepts of Internet and Embedded agent.
- To obtain basic knowledge distributed computing using Java.

Course Outcomes

After successful completion of this course, the students should be able to

CO1: Understand network protocol layers and explain the specific role of each.

CO2: Complete design of an embedded system with functional requirements for hardware and software components 3.Develop software systems for measurement of embedded system operating characteristics (for example, latency, data transport rate, error rate).

CO3: Completed a subsystem and integrate this with a complete system to perform a complex task involving networked, mobile, embedded systems.

	CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak											
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S		M		W			M	S		M	
CO2	S	M			M	S					M	
CO3	S									M		

UNIT-I

THE HARDWARE INFRASTRUCTURE 9

Board band transmission facilities – open interconnection standards – local area networks – wide area networks – network management – network security – cluster computers.

UNIT-II

SOFTWARE ARCHITECTURE 9

client - server architecture - challenges - design methodology – intranets and group ware – hardware and software for intranet – group and features – network as a computer – the internet – IP addressing – internet security – open systems – concepts and reliability.

UNIT-III

INTERNET CONCEPTS 9

Capabilities and limitations of the internet – interfacing internet server applications to corporate databases HTML and XML web page design and the use of the active components.

UNIT-IV

DISTRIBUTED COMPUTING USING JAVA 9

10 streaming – object serialization – networking – threading – RMI – multicasting – distributed databases – embedded java concepts – case studies.

UNIT-V

EMBEDDED COMPUTING ARCHITECTURE 9

Synthesis of the information technologies of distributed embedded systems analog/digital co – design – optimizing functional distribution in complex system design – validation and fast prototyping of multiprocessor system – on – chip – a new dynamic scheduling algorithm for real –time multiprocessor systems.

Total Periods: 45 Hours

References

1. Dietel & Dietel, "Java How To Program", Prentice Hall 1999
2. Sapemullender,"Distributed Systems", Addison-Wesley, 1993
3. George Coulouris And Jean Dollimore,"Distributed Systems – Concepts And Design", Addison – Wesley 1998
4. "Architecture and Design Of Distributed Embedded Systems", Edited By Berndkleinjohann C- Lab, University Paderhorn, Germany, Kluywer Academic Publishers, Boston, April 2001, 248pp.

MES005 DESIGN OF DIGITAL CONTROL SYSTEM 3 0 0 3

Course Objectives

- To learn the fundamental principles of feedback control and dynamic systems
- To acquire the concepts of Optimal Control Systems and Digital Control Systems
- To Model and control hybrid systems
- To learn how to perform the stability analysis of Feedback Control Systems

Course Outcomes

After successful completion of this course, the students should be able to

CO1: Be familiar with The Design of Feedback Control Systems employing the previously learnt techniques such as the Bode Diagram, and the Root Locus method.

CO2: Become familiar with issues faced in sampling, digital data and discrete time systems.

CO3: Acquire the concepts of the Stability in the Frequency Domain employing The Nyquist Criterion, the Relative Stability, and Time Domain Performance Criteria in the Frequency Domain.

CO4: able to apply advanced technical knowledge in multiple contexts

CO5: able to understand and design advanced electronics systems (Analog and Digital Systems) and conduct experiments, analyze and interpret data

	CO/PO Mapping
	(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S		M		W			M	S		M	
CO2	S	M			M		S	M			M	
CO3	S					S	W			M		
CO4	M	M		M	W		M	W	S	M		
CO5	M				M		S	M				

UNIT-I INTRODUCTION 9

Effect of sampling – review of continuous control systems – modeling – control design - time and frequency domain techniques.

UNIT-II DISCRETE TIME SYSTEMS 9

Analysis of discrete time systems – difference equations – Z – transforms – time and frequency response – sample data systems – sample and hold – sampling and extrapolation – A/D and D/A conversion of systems.

UNIT-III DESIGN USING TRANSFORM AND STATE SPACE TECHNIQUES 9

Methods of discretisation – comparison – direct design frequency response methods state space design – controllers/estimator design – controllability and observability

UNIT-IV QUANTIZATION EFFECT AND SAMPLE RATE SELECTION 9

Analysis of round off error – parameter round off – limit cycles and dither – sampling theorem limit – time response and smoothness – sensitivity to parameter variation – cement noise and analyzing filter – multi – rate sampling.

UNIT-V COMPUTER BASED CONTROL 9

Selection of processers – mechanization of control algorithms – PID control law – merits and demerits of various algorithms – applications to temperature control – design of DD systems – stepper motors and motor controllers and stepper motor control systems.

Total Periods: 45 Hours

Reference Books:

1. GopalM,"digital control engineerinfg", wiley eastern, 1989
2. K. ogata,"discrete time control systems", PHI 1987
3. Frosytheand W. goodaaaR.N,"digital control ", McMillman,1991

MES006 CRYPTO ANALYTIC SYSTEMS 3 0 0 3

Course Objectives:

- To know about various encryption techniques.
- To understand the concept of Public key cryptography.
- To study about message authentication and hash functions

- To impart knowledge on Network security
- To learn the basic concepts of system level security

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: Classify the symmetric encryption techniques.

CO2: Illustrate various Public key cryptographic techniques.

CO3: Evaluate the authentication and hash algorithms.

CO4: Discuss authentication applications

CO5: Summarize the intrusion detection and its solutions to overcome the attacks.

	CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak											
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S		M		W			M	S		M	
CO2	S	M			M	S					M	
CO3	S									M		
CO4	M	M		M	M	S		M	S	M		
CO5	M				M			M				

UNIT-I

SECURITY PROBLEM **9**

Security problem in computing – characteristics of computers in intrusion – kinds of security preaches – points of security vulnerability – methods of defense – controls – effectiveness of controls – plan of attack encryption

UNIT-II

CRYPTOGRAPHY **9**

Basic encryption and decryption – mono alphabetic ciphers – polyalphabetic submission – transpositions – fractional Morse – stream and block ciphers-characteristics of good ciphers – secure encryption systems – public key system – single key system – data encryption standard – rivest – Shamir – Adelman (RSA) encryption

UNIT-III

ROLE OF OPERATING SYSTEM **9**

Security involving programs and operating system – information access problems – program development controls – operating system controls – operating system controls in use of programs administration controls – protection services for users of operating system – protected objects and method of protection – file protection mechanism – user authentication.

UNIT-IV

DATABASE AND NETWORK SECURIY **9**

Databases and network security – security requirements for data base – reliability and integrity – sensitive data – interference problem – multilevel data bases – network security issues – encryption in networking – access control – user authentication – local area networks – multi level security of network.

UNIT-V

COMMUNIOCATION AND SYSTEM SECURITY 9

Communication and system security – communication characteristics – communications media – loos of integrity – wire tapping – electronic mail security IP security – WEB security – intruders – viruses – worms firewalls – standards.

Total Periods: 45 Hours

Text books

1. William Stallings Cryptography And Network Security Principles And Practice, PHI 1998
2. Charles, P. Pleeger, Security In Computing, PHI, 1998

Reference Books

1. Hans, Information And Communiocation Security, Springer Verlag, 1998
2. Simonds, Network Security, McGraw Hill, 1998
3. Derek Atkins, Internet Security, Techmedia, 1998
4. Kernel Texplan, Communication Network Management, PHI,1992.

MES007 INTELLIGENT EMBEDDED SYSTEMS 3 0 0 3

Course Objectives:

- The course aims to give the student an opportunity to integrate theoretical and practical competence relevant for research and development of embedded and intelligent systems.

Course Outcomes

After successful completion of this course, the students should be able to

CO1: Program an embedded computer implementing functions for situation and position estimation, motor control and wireless communication in a distributed system.

CO2: Apply and use sensors and techniques for calibration altering and combination of signals from different sensors.

CO3: Use skills in own specialization area in project work and cooperate with other specialists.

CO4: Use modern engineering tools necessary for integrating software and hardware components in embedded system designs.

	CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak											
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S		M		W			M	S		M	
CO2	S	M		S	M	S					M	

CO3	S		S	W						M		
CO4	M	W		M	M	S		M	S	M		
CO5	M	M		S	M			M				

UNIT-I INTRODUCTION **9**

Overview of agent based intelligent inhabited environments such as intelligent buildings introduction to the embedded – internet. Embedded agents and intelligent inhabited environments using examples from notable work-topologies for intelligent inhabited environments – brief review of control methods – behavior based embedded-agent – Agent and system intelligence (e.g. Reactivity versus and deliberation)

UNIT-II EMBEDDED_AGENT DESIGN **9**

Embedded – agent design criteria and issues – considerations of various solutions, in particular behavior based methods, which are the prime focus of the course behavior based agent (BBA) mechanism implementing reactive functionality in embedded agents – knowledge in embedded agents – behavior based agents (BBA) mechanisms for implementing deliberative functionality in embedded agents

UNIT-III MULTIEMBEDDED AGENTS **9**

Overview of multi embedded – agents infrastructure including networking standards for intelligent buildings – embedded agent co-ordination, mechanisms and bench marks embedded agents

UNIT-IV HUMAN-MACHINE **9**

HMI interfacing issues in intelligent inhibited environments and their relationship to cognitive disappearance – individually commercial issues – technical design consequences arising from social issues such as privacy, Asimov –like rules

UNIT-VHIGH-END APPLICATIONS **9**

Case studies self-directed deep space probes – robotic soccer teams- underwater submarines – acrobatic helicopters and mobile robots.

Total Periods: 45 Hours

Reference Books

1. ArkinR.C,"Behavior –Based Robotics", The MIT Press, 1998
2. Rievski. G,"Mechantronics" Designing Intelligent Machines" Butterworth Heinmann, 1995
3. Steels, l and r, "The Artificial Life Route To Artificial Intelligence" Building Embodied Situated Agents", Lawrence Erlbaum, 1995.

MES008 REAL TIME OPERATING SYSTEMS 3 0 0 3

Objectives:

- The aim of the course is to impart the concepts related to operating systems concepts and to discuss about RTOS application domains.
- To study about client server model- distributed file systems.
- To learn about synchronization control blocks
- To know about comparison and study of various RTOS like QNX-VX works
- To understand RTOS for image processing

Course Outcomes:

After successful completion of this course, the students should be able

CO1: To understand and review about different operating system

CO2: To understand about networking and distributed operating system

CO3: To understand about real time models and languages

CO4: To understand about real time kernel

CO5: To know about various application domains in RTOS.

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S		M			W	S				S	S
CO2		M		W	S		M		S	M		S
CO3			S		M			S	W		S	
CO4	M			M			W		M	W		S
CO5							M		S	M	S	S

UNIT – I **9**

REVIEW OF OPERATING SYSTEMS

Basic Principles – System calls – Files – Processes – Design and Implementation of Processes – Communication between Processes – Operating System Structures.

UNIT – II **9**

DISTRIBUTED OPERATING SYTEMS

Topology – Network types – communication – RPC- client server model- distributed file systems- design strategies.

UNIT – III **9**

REAL TIME MODELS AND LANGUAGES

Events based – process based and graph based models – petrinet models – real time languages – RTOS tasks – RT scheduling – interrupt processing – synchronization control blocks – memory requirements.

UNIT – IV **9**

REAL TIME KERNEL

Principles – design issues – Polled loop systems - RTOS porting to a target – comparison and study of various RTOS like QNX-VX works – PSOS – C executive - Case studies.

UNIT – V **9**

RTOS APPLICATION DOMAINS

RTOS for image processing - Embedded RTOS for voice over IP – RTOS for voice over IP – RTOS for fault tolerant applications – RTOS for control systems.

Total Periods: 45 Hours

References

1. Herma K, " Real Time Systems – Design for distributed Embedded Applications ",Kluwer Academic, 1997.
2. Charles Crowly, "Operating System – A design oriented approach" McGraw Hill, 1997.
3. R.J.A Bhur, D.L. Bailey, "An introduction to Real Time Systems', PHI 1999.
4. C.M. Krishna, Kang G Shin, "Real time systems", McGraw Hill, 1997

MES009 ADVANCED MICROPROCESSORS 3 0 0 3

Course objectives:

- To expose the students to the fundamentals of microprocessor architecture.
- To introduce the advanced features in microprocessors and microcontrollers.
- To enable the students to understand various microcontroller architectures.

Course outcomes:

After successful completion of this course, the students should be able to

CO1: The student will be able to work with suitable microprocessor/microcontroller for a specific real world application.

CO2: Understand the generalized architecture of advanced microprocessors and advanced microcontrollers.

CO3: Develop algorithm/program of the advanced microcontrollers for a particular task.

CO4: Interface advanced microcontrollers with external peripherals.

CO5: Students can understand the evaluation of microprocessors and microcontroller.

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1			S	M	M		S					
CO2	S	M	M			S	W					

CO3				S	W		M					
CO4		S	W		M		S					
CO5	M											

UNIT – I **9**

Evaluation of 16/32 Bit Processor – 8086 Processor: Architecture – Programming Model – Memory Organization – Interrupt Structure – Instruction Set.

UNIT – II **9**

80X 86 PROCESSOR FAMILIES: 80286 Processor – Functional Block Diagram – Memory Organization – Modes of Operation – Real and Protected Modes – Address Translation Techniques – Virtual Memory.

UNIT – III **9**

80386 Processor : Basic Programming Model – Memory Organization – Data Types Instruction Set, Addressing Modes – Address translation – Interrupts – Assembly Language Programming. 80486 Processor : Architecture and Programming Model – Pentium Processor Architecture.

UNIT – IV **9**

680X0 Processor Family : 68020 Processor : Functional blocks – Programmers model – Data types Organisation – Instruction Set – Exception Processing – Cache Memory – Virtual Memory – Memory Management Unit.

UNIT – V **9**

68030 Processor : Block Diagram – Programming Model – On Chip Memory Management Unit – Read Write Timing Diagram – Addressing Modes Instruction Set. RISC Processor : Features of RISC Processor – Typical RISC Processor Architecture.

Total Periods : 45 Hours

References:

1. Mohammed Rafiquzzman, "Microprocessos and Microcomputer Based System Design", Universal Book Stall, New Delhi, 1990.
2. Barry B Bery, "The Intel Microprocessor 8086/8088, 80186/80188, 80286, 80386, 80486, Pentium and Pentium Pro – Processor Architecture, Programming and Interfacing",Prentice Hall of India, 4th Edition, 1997.
3. Intel, "Microprocessors, Vol-I &Vol-II", Intel Corporation, USA, 1992.
4. Intel Ciminera and Advance Voltage "Advanced Microprocessor Architecture", Addison Wesley, USA, 1987.

MES010 ARTIFICIAL INTELLIGENCE AND EXPERT SYSTEM 3 0 0 3

Course Objectives:

- AI programs that achieve expert-level competence in solving problems in task areas by bringing to bear a body of knowledge about specific tasks are called knowledge-based or expert systems.
- The term expert systems is reserved for programs whose knowledge base contains the knowledge used by human experts, in contrast to knowledge gathered from textbooks or non-experts.
- More often than not, the two terms, expert systems (ES) and knowledge-based systems (KBS), are used synonymously.
- The area of human intellectual endeavor to be captured in an expert system is called the task domain. Task refers to some goal-oriented, problem-solving activity.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: Concepts of Artificial Intelligence and Expert System Concepts. Examine methods that have emerged from both fields

CO2: Explain the various current mirror circuits and analyze differential amplifier with active load.

CO3: Analyze and design a fuzzy logic system using fuzzy logic tool box.

CO4: Analyze and design a neural network system using neural network toolbox.

CO5: Analyze and design a rule-based expert system.

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1			S	M				M		S		
CO2	S	M	M		S				S	W		
CO3				S	W		M	W		M		
CO4		S	W		M			M		S		
CO5	M											

UNIT-I INTRODUCTION TO ARRTIFICIAL INTELLIGENCE 9

Overview of Al-general concepts- problem spaces and search- Search techniques –Bfs, DFS-Heuristic search techniques

UNIT-II KNOWLEDGE REPRESENTATION 9

Knowledge- general concepts – predicate logic – representing simple fact- instance and ISA relationships- Resolution – Natural deduction

UNIT-III KNOWLEDGE ORGANISATION AND MANIPULATION 9

Procedural versus Declaration knowledge – forward vsBackward reasoning- matching techniques- control knowledge/strategies – symbol reasoning under uncertainty- introduction to non –monotonic- reasoning- logic for monotonic reasoning

UNIT-IV PERCEPTRON- COMMUNICATION AND EXPERT SYSTEMS 9

Natural language processing – pattern recognition- visual image understanding – Expert system architecture

UNIT-V KNOWLEDGE ACQUISTION 9

Knowledge acquisition- general concepts – learning – learning by introduction- Explanation based learning

Total periods :45 Hours

Texts books:

1. Elaine Rich and kelvin Knight, Artificial Intelligence, Tata mcgraw Hill, New Delhi
2. Stuart Russell and peter Norvig , Artificial Intelligence : A modern approach, Prentice Hall,1995

References books:

1. Nilson N. J.Principles of Artificial Intelligence ,SpringrVerlag – Bergin,1980.
2. Pattrson, Introdution of Artificial intelligence and Expert systems prentice Hall of India, New Delhi,1990

MES011 ADVANCED DIGITAL SIGNAL PROCESSING 3 0 0 3

Objectives:

- To learn about random signal processing
- To know about spectrum and linear estimation.
- To know about adaptive filters
- To understand the concepts related to multirate digital signal processing.
- To study about Decimation by an integer factor

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: To learn about random signal processing and there algorithms

CO2: To know about spectrum and linear estimation for various methods of spectrum analyser

CO3: To know about adaptive filters linear estimation and their premitives.

CO4: To understand the concepts related to adaptive filters digital signal processing.

CO5: To understand different amplifiers in low signal.

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak												
COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S		M			W						S
CO2		M		W	S							S
CO3			S		M	M		S	M			S

CO4	M			M			S	W				
CO5						W		M	W			S

UNIT-I DISCRETE RANDOM SIGNAL PROCESSING 9

Discrete Random Processes,Expectations,Variance,Co-variance,Scalar product, Energy of Discrete Signals-Parseval's Theorem, Wiener Khintchine Relation-Power Spectral Density-Periodogram-Sample Autocorrelation-Sum Decomposition Theorem, Spectral Factorization Theorem-Discrete Random Signal Processing by Linear Systems-Simulation of White Noise-Low Pass filtering of white noise.

UNIT-II SPECTRUM ESTIMATION 9

Non-Parametric Methods–Correlation Method–Co-Variance Estimator-Performance Analysis of Estimator-Barlett Spectrum Estimation –Welch Estimation-Model Based Approach-AR,MA,ARMA Signal Modeling –Parameter Estimation using Yule-Walker Method.

UNIT-III LINEAR ESTIMATION AND PREDICTION 9

Maximum likelihood criterion-efficiency of estimator-least mean squared error criterion-Wiener filter –Discrete Wiener Hoff Equation–Recursive estimators–Kalman filter–linear prediction, prediction error whitening filter, inverse filter-Levinson recursion, Lattice realization and Levinson recursion algorithm for solving Toeplitz system of equations.

UNIT-IVADAPTIVE FILTERS 9

FIR adaptive filters-Newton's steepest descent method-adaptive filter based on steepest descent method-Widrow Hoff LMS adaptive algorithm-Adaptive channel equalization-Adaptive echocarcellor-Adaptive noise cancellation –RLS adaptive filter-Exponentially weighted RLS –Sliding window RLS –Simplified IIRLMS adaptive filter.

UNIT-V MULTIRATE DIGITAL SIGNAL PROCESSING 9

Mathematical description of sample rate-interpolation and Decimation-continuous time model direct digital approach-Decimation by an integer factor–interpolation by an integer factor-Single and multistage realization-poly phase realization-Application to Sub band coding-Wavelet transform and filter bank implementation of wavelet expansion of signals.

Total Periods :45 Hours

Textbooks:

1. Monson.H.Hayes, Statiscal Digital Processing and Modelling, John Wiley and Sons.INC, New York.1996.

References:

1. Sophocles J.Orfanidis, OptimumSignal Processing, McGraw Hill.1990.
2. John.G.Proakis, Dimitris G.Manofakis.Digital Signal Processing Prentice Hall of India, 1995.

MES012 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING 3 0 0 3

Course Objectives:

- To understand the difference between the pipeline and parallel concepts.
- To study the various types of architectures and the importance of scalable architectures.
- To study the various memories and optimization of memory.
- To know about Parallel and scalable architectures
- To study about environments, UNIX, MACH and OSF/1 for parallel computers.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: To understand the performances and measures for VLSI.

CO2: To understand the various types of architectures.

CO3: To study the various memories and optimization of memory.

CO4: Compare and evaluate the performance of various architectures

CO5: Analyze the requirements of large systems to select and build the right infrastructure.

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S		M			W	S					S
CO2		M		W	M		S	M				
CO3			S			S	W					**S**
CO4	M			M	W		M	W				**S**
CO5					M		S	M				

UNIT-I THEORY OF PARALLESISM –PART-I 9

Parallel computer models-the state of computing, Multiprocessor and Multicomputer and Multivectors and SIMD computers, PRAM and VLSI mode Architectural development tracks .Program and properties Conditions of parallelism.

UNIT-II THEORY OF PARALLELISM –PART-II 9

Program partitioning and scheduling, Program flow mechanism, System inter connect architecture, Principles of scalable performance–performance matrices and measures, Parallel processing application speedup performance laws, scalability analysis and approaches.

UNIT-III HARDWARE TECHNOLOGIES 9

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory-backplane bus systems, cache memory organizations, shared memory organization, sequential and weal consistency model.

UNIT-IV PIPELINING AND SUPERSCALAR TECHNOLOGIES 9

Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivectors and SSIMD Computers, Scalable Multithread and dataflow architectures.

UNIT-V SOFTWARE AND PARALLEL PROCESSING 9

Parallel models,Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

Total Periods: 45 Hrs

References:

1. Kai Hawang, "Advanced Computer Architecture", McGraw Hill international, 1993.
2. William Stallings, "Computer Organization and Architecture", Macmillan Publishing Company, 1990.

M.J.Quinn, "Designing Efficient Algorithms for Parallel Computer", McGraw Hill International1994.

MES0013 DESIGN OF SEMICONDUCTOR MEMORIES 3 0 0 3

Objectives:

- To study the architectures for SRAM and DRAM
- To know about various non-volatile memories.
- To study the fault modeling and testing of memories for fault detection.
- To learn the radiation hardening process and issues for memory.
- To know about Ferroelectric Random Access Memories (FRAMs).

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: Design Memory Structures.

CO2: Decide the type of memory for a specific application.

CO3: Describe the smartness in the circuits used for memories.

CO4: Design the architectures of Static and Random Access, Nonvolatile memories.

CO5: Evaluate the fault modeling and testing procedures for memory circuit.

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S	S		S			M		S	M	S
CO2	M		S	M	S				S	W		S
CO3		S	W		S			W		M	W	S
CO4	W		M	W	S			M		S	M	S
CO5	M		S	M	S			S	M		S	S

UNIT-I RANDOM ACESS MEMORY TECHNOLOGY 9

Static Random Access Memories(SRAM) SRAM Cell Structure-MOS SRAM Architecture-MOS SRAM Cell and Peripherals Circuit Operation – Bipolar SRAM Technologies –Silicon On Insulator (Sol) Technology – Advanced SRAM Architecture and Technologies – Application

Specific SRAMs Dynamic Random Access Memoirs(DRAMs) DRAM Technology Development – CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures-BICMOS DRAMs – Soft Error Failure in DRAMs – Advanced DRAM Designs and Architecture – Application Specific DRAMs.

UNIT-II NON VOLATILE MEMORIES 9

Mask Read Only Memories(ROMs)-High Density ROMs-Programmable Read Only Memories(PROMs)-Bipolar PROMs CMOS PROMs-Erasable (UV) – Programmable Read Only Memories(EPROMs) - Floating – Gate EPROM Cell-One Time Programmable (OTP) EPROMs -Electrically Erasable PROMs(EEPROMs) – EEPROM Technology and Architecture – Non Volatile SRAM – Flash Memories (EPROM or EEPROM)

UNIT-III MEMORY FAULTS MODELLING, TESTING AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE 9

RAM Fault, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault modeling and Testing-Application Specific Memory Testing

UNIT-IVSEMICONDUCTOR MEMORY RELIABILITY AND RANDOM EFFECTS 9

General Reliability Issues-RAM Failure Modes and Mechanism - Nonvolatile Memory Reliability – Reliability Modeling and Failure Rate Prediction – Design for Reliability – Reliability Test Structures – Reliability Screening and Qualification. Radiation Effects-Single Event Phenomenon (SEP) – Radiation Hardened Memory Characteristics – Radiation Hardness Assurance and Testing – Radiation Dosimettry - Water Level Radiation Testing and Test Structures.

UNIT–VADVANCED MEMORY TECHNOLOGIES AND HIGH DENSITY MEMORY PACKAGING TECHNOLOGICS 9

Ferroelectric Random Access Memories (FRAMs) – Gallium Arsenide (GaAs) FRAM – Analog Memories Magneto Resistive Ferroelectric Random Access Memories (MRAMS) – Experimental Memory Devices Memory Hybrids and MCMs (2D – Memory Stacks and MCMs 3D) – Memory MCM Testing and Reliability Issues – Memory Cards – High Density Memory Packing Feature Directions.

Total periods: 45 Hrs

Text Books:

1. Ashok K. Sharma, “Semiconductor Memories Technology, Testing, and Reliability”, Prentice Hall of India Limited. New Delhi 1997.

MES014 VLSI ARCHITECTURE AND DESIGN METHODOLOGIES 3 0 0 3

Course Objectives:

- To give an insight to the students about the significance of CMOS technology and fabrication process.

- To teach the importance and architectural features of programmable logic devices.
- To introduce the ASIC construction and design algorithms
- To teach the basic analog VLSI design techniques.
- To study the Logic synthesis and simulation of digital system with Verilog HDL.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: To understand about the advanced topics in Boolean algebra.

CO2: To know about analog and high speed VLSI.

CO3: To know in detail about programmable ASICs and its interconnects.

CO4: To understand about programmable ASIC its logic synthesis, simulation and testing of VLSI circuits

CO5: To understand about simulation and testing of VLSI circuits

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	M		S	M		M		S	M		S	M
CO2		S	W		S		S	W		S	W	
CO3	W		M	W		W		M	W		M	W
CO4	M		S	M		M		S	M		S	M
CO5	S	S	S		S			S	M		S	S

UNIT-I INTRODUCTION **9**

Overview of a Digital VLSI design Methodologies- Trends in IC Technology advanced Boolean algebra- Shannon's expansion theorem- consensus theorem – Octal designation-Run Measure – Buffer gates- Gate Expander- Reed Muller expansion- Synthesis of multiple output combinational logic circuits by product map method- Design of Static hazard free and dynamic hazard free logic circuits.

UNIT-II ANALOG VLSI AND HIGH SPEED VLSI **9**

Introduction to analog VLSI- Realisation of Neural Networks and switched capacitors filters- sub- micron Technology and GaAs VLSI technology.

UNIT-III PROGRAMMABLE ASICS **9**

Antifuse- Static RAM-EPROM and EEPROM technology – PREP bench marks – Actel ACT – Xilinx LCA- Altera FLEX- Altera MAX DC & AC inputs and outputs – clocks and power inputs – Xilinx I/O blocks.

UNIT-IV PROGRAMMABLE ASIC DESIGN SOFTWARE **9**

Actel ACT – Xilinx LCA- Xilinx EPLD - Altera MAX 5000 & 7000 – Altera Max 9000 – Design Systems – Logic synthesis – half gate ASIC – Schmatic entry – low level design language – PLA tools – EDIF – CFI design representation.

UNIT-V LOGIC SYNTHESIS , SIMULATION AND TESTING 9

Basic features of VHDL language for behavioral modeling and simulation – Summary of VHDL data types – Dataflow and structural modeling – VHDL and logic Synthesis – types of simulation – Boundary scan Test – fault Simulation – Automatic test Pattern Generation.

Total Periods: 45 Hours

References:

1. Willam I. Fletcher " An Engineering Approach to Digital Design" Prentice Hall of India 1996.
2. Amar Mukherjee, "Introduction to NMOS and CMOS VLSI System Design". Prentice Hall of India 1986.
3. M.J.S. Smith "Application – Specific Integrates Circuits ", Addison Wesley Longman Inc. 1997.
4. Fedrick J. Hill and Gerald R. Peterson, " Computer Aider Logical Design with Emphasis on VLSI

MES015 INTRODUCTION TO VLSI DESIGN 3 0 0 3

Objectives:

- To understand the concepts of MOS transistors operations and their AC , DC characteristics.
- To know the fabrication process of CMOS technology and its layout design rules.
- To know the concepts of power estimation and delay calculations in CMOS circuits.
- To learn about the VLSI circuit components and physical design.
- To study the concepts of Verilog in designing digital logic circuits.

Course Outcomes:

After successful completion of this course, the students should be able to

CO1: Design layout and schematic and analysis digital logic gates

CO2: Simulate different logic gates using industry standard software CAD tools Cadence

CO3: Explain the purpose and applications of CMOS technology

CO4: Familiar with Digital Integrated Circuits and System Building Blocks

CO/PO Mapping

(S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak

COs	Programme Outcomes(POs)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	S	S	S		S			S	M		S	S
CO2	M		S	M		S		M		S	M	
CO3		S	W		S	W			S	W		S

CO4	W		M	W		M		W		M	W	
CO5	M		S	M		S		M		S	M	

UNIT – I MOS TECHNOLOGY AND CIRCUITS 9

MOS Technology and VLSI, Process parameters and consideration for BJT, MOS and CMOS, CMOS logic, MOS transistor theory , Enhancement mode transistor action, Ideal I-V characteristics, DC transfer characteristics, Threshold voltage, Body effect,Design equations, Second order effects. MOS models and small signal AC characteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance model.

UNIT –II CMOS CIRCUITS DESIGN PROCESS 9

CMOS fabrication, P -Well process, N -Well process, twin - tub process, MOS layers stick diagrams and Layout diagram, Layout design rules, Latch up in CMOS circuits, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III CIRCUIT CHARACTERIZATIONAND PERFORMANCE ESTIMATION9

Resistance estimation, Capacitance estimation, Inductance, switching characteristics,transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT – IV VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN 9

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits,Ripple carry adders,Carry look ahead adders,High-speed adders, Multipliers. Physical design – Delay modelling ,cross talk, floor planning, power distribution. Clock distribution.

UNIT V SPECIFICATION USING VERILOG HDL 9

Basic concepts- identifiers- gate primitives, gate delays, operators, timing controls, procedural assignments conditional statements, Data flow and RTL, structural gate level switch level modeling, Design hierarchies, Behavioral and RTL modeling, Test benches, Design of decoder, equality detector, comparator, priority encoder, half adder, full adder, Ripple carry adder, D latch and D flip flop

Total Periods: 45 Hours

References:

1. Douglas A. Pucknell and Kamran Eshraghian, “Basic VLSI Design Systems and Circuits”, Prentice Hall of India Pvt. Ltd., 1995.
2. Wayne Wolf, ”Modern VLSI Design”, 2nd Edition, Prentice Hall 2002.
3. Amar Mukherjee, “Introduction to NMOS and CMOS VLSI System Design,” Prentice Hall,
4. Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.

5. John P.Uyemura “Introduction to VLSI Circuits and Systems”, John Wiley &

RESEARCH METHODOLOGY

Objectives

- To Get adequate knowledge about research concepts
- To describe mathematical modeling and simulation
- To understand experimental modeling
- To get knowledge about the interpretation of result

Course Outcomes after successful completion of this course, the students should be able to

CO 1: To describe research concepts.

CO 2: To Get adequate knowledge about mathematical modeling

CO 3: To describe experimental modeling

CO 4: To understand analysis of results.

CO 5: To know about report writing

CO/PO Mapping (S/M/W indicates strength of correlation) S-Strong, M-Medium, W-Weak							
COs	Programme Outcomes(POs)						
	PO1	PO2	PO3	PO4	PO5	PO6	PO7
CO1	S	M				M	M
CO2	S	M				M	M
CO3	S	M				M	M
CO4	S	M				M	M
CO5	S	M				M	M

1. RESEARCH CONCEPTS 9

Concepts, meaning, objectives, motivation, types of research, approaches, research (Descriptive research, Conceptual, Theoretical, Applied & Experimental).

Formulation of Research Task – Literature Review, Importance & Methods, Sources, quantification of Cause Effect Relations, Discussions, Field Study, Critical Analysis of Generated Facts, Hypothetical proposals for future development and testing, selection of Research task.

2. MATHEMATICAL MODELING AND SIMULATION 9

Concepts of modeling, Classification of Mathematical Models, Modeling with Ordinary differential Equations, Difference Equations, Partial Differential equations, Graphs, Simulation, Process of formulation of Model based on Simulation.

3 EXPERIMENTAL MODELING 9

Definition of Experimental Design, Examples, and Single factor Experiments, Guidelines for designing experiments. Process Optimization and Designed experiments, Methods for study of response surface, determining optimum combination of factors, Taguchi approach to parameter design.

4 ANALYSIS OF RESULTS 9

Parametric and Non-parametric, descriptive and Inferential data, types of data, collection of data (normal distribution, calculation of correlation coefficient), processing, analysis, error analysis, different methods, analysis of variance, significance of variance, analysis of covariance, multiple regression, testing linearity and non-linearity of model.

5 REPORT WRITING 9

Types of reports, layout of research report, interpretation of results, style manual, layout and format, style of writing, typing, references, tables, figures, conclusion, appendices.

TOTAL: 45

TEXT BOOKS

1. Wilkinson K. L, Bhandarkar P. L, „Formulation of Hypothesis", Himalaya Publication.
2. Schank Fr.,"Theories of Engineering Experiments", Tata Mc Graw Hill Publication.

REFERENCE BOOKS

1. Douglas Montgomery, "Design of Experiments", Statistical Consulting Services, 1990.
2. Douglas H. W. Allan, "Statistical Quality Control: An Introduction for Management", Reinhold Pub Corp, 1959.
3. Cochran and Cocks, "Experimental Design", John Willy & Sons.
4. John W. Besr and James V. Kahn, „Research in Education", PHI Publication.
5. Adler and Granovky, "Optimization of Engineering Experiments", Meer Publication.
6. S. S. Rao, „Optimization Theory and Application", Wiley Eastern Ltd., New Delhi, 1996.