CURRICULUM – SYLLABUS (R2015)

CHOICE BASED CREDIT SYSTEM
M.TECH. VLSI DESIGN
(FULL TIME)
I – IV SEMESTERS

SEMESTER-I						
Code	**Category**	**Subject Name**	**L**	**T**	**P**	**C**
Theory						
MMA101	PM	Applied Mathematics for Electronics Engineers	3	1	0	4
MVL101	PC	Solid state device modeling and simulations	3	0	0	3
MAE102	PC	Advanced Digital System Design	3	0	0	3
MVL102	PC	Introduction to VLSI Design	3	0	0	3
MVL1E1	PE	Professional Elective-I	3	0	0	3
Practical						
MVL1L1	PC	VLSI Design lab – I	0	0	4	2
Total No. of Contact Hours: 20					**Total Credits: 18**	

SEMESTER-II						
Code	**Category**	**Subject Name**	**L**	**T**	**P**	**C**
Theory						
MAE201	PC	Analysis and Design of Analog Integrated circuits	3	0	0	3
MVL201	PC	Computer Aided design of VLSI Circuits	3	0	0	3
MVL202	PC	Low Power VLSI	3	0	0	3
MVL2E2	PE	Professional Elective-II	3	0	0	3
MVL2E3	PE	Professional Elective-III	3	0	0	3
Practical						
MVL2L2	PC	VLSI Design Lab –II	0	0	4	2
Total No. of Contact Hours: 20					**Total Credits: 17**	

SEMESTER-III

Code	Category	Subject Name	L	T	P	C
Theory						
MVL3E3	PE	Professional Elective-IV	3	0	0	3
MVL3E4	PE	Professional Elective-V	3	0	0	3
MVL3E5	OE	Open Elective - I	3	0	0	3
MVL3P1	PR	Project work phase-I	0	0	12	6
Total No. of Contact Hours: 21					**Total Credits:15**	

SEMESTER-IV						
Code	**Category**	**Subject Name**	**L**	**T**	**P**	**C**
MVL4P2	PR	Project work phase-II	0	0	24	12
Total No. of Contact Hours: 24					**Total Credits: 12**	

OVERALL CREDIT FOR THE PROGRAMME - 62

LIST OF ELECTIVES

PROFESSIONAL ELECTIVE – I(PE-I)

Code No.	Course Title	L	T	P	C
MVL001	CMOS VLSI DESIGN	3	0	0	3
MVL002	VLSI SIGNAL PROCESSING	3	0	0	3
MVL003	ANALOG VLSI DESIGN	3	0	0	3

PROFESSIONAL ELECTIVE – II(PE-II)

Code No.	Course Title	L	T	P	C
MVL004	SYSTEM ON CHIP DESIGN	3	0	0	3
MVL005	DESIGN OF SEMICONDUCTOR MEMORIES	3	0	0	3
MVL006	VLSI ARCHITECTURE AND DESIGN METHODOLOGIES	3	0	0	3

PROFESSIONAL ELECTIVE – III(PE-III)

Code No.	Course Title	L	T	P	C
MVL007	SUBMICRON VLSI DESIGN	3	0	0	3
MVL008	TESTING OF VLSI CIRCUITS	3	0	0	3
MVL009	NANOSCALE DEVICES AND CIRCUIT	3	0	0	3

PROFESSIONAL ELECTIVE – IV(PE-IV)

Code No.	Course Title	L	T	P	C
MVL014	ADVANCED DIGITAL SIGNAL PROCESSING	3	0	0	3
MVL013	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN	3	0	0	3
MVL010	OPTIMIZATION TECHNIQUES IN VLSI DESIGN	3	0	0	3

PROFESSIONAL ELECTIVE – V(PE-V)

Code No.	Course Title	L	T	P	C
MVL011	VLSI for Wireless Communication	3	0	0	3
MVL012	Computer Architecture and Parallel Processing	3	0	0	3
MVL015	Real Time Operating System	3	0	0	3

OPEN ELECTIVE – I(OE-I)

Code No.	Course Title	L	T	P	C
MED102	EMBEDDED SYSTEMS	3	0	0	3
MED201	ASIC DESIGN	3	0	0	3
MST070	RESEARCH METHODOLOGY	3	0	0	3

SUMMARY OF CURRICULUM STRUCTURE AND CREDIT & CONTACT HOUR DISTRIBUTION

S. No.	Sub Area	Credit AS per Semester				No. of Credit	% of credit
		I	II	III	IV		
1	Professional Mathematics (PM)	4				4	6.06
2	Professional Core (PC)	11	11			24	36.36
3	Professional Electives (PE)	3	6	6		15	22.72
4	Open Electives (OE)			3		3	4.54
5	Project Work, Seminar, Internship, Term Paper, etc. (PR)			6	12	20	30.30
6	Total Credit	18	17	15	12	62	100
7	Total Contact Hour	20	20	21	24	85 Hrs	-

Course Code MMA101	**Course Name:** Applied Mathematics for Electronic Engineers	**L**	**T**	**P**	**C**
	Total Contact Hours:60	3	1	0	4
	Prerequisite: ENGINEERING MATHEMATICS				
	Course Designed by : Dept of Mathematics				

OBJECTIVES

To apply all taught techniques to unseen problems, and queuing is a major branch of optimization, Random variable compute and interpret means, correlation/covariance, PERT and CPM chart is mainly used for documenting the data(visually) on projects.

COURSE OUTCOMES (COs)

CO1	The student will learn to analyse and solve the fundamental problems with prescribed conditions in simple cases.
CO2	The student will learn to understand how signals, systems, inference combine in prototypical tasks of communication.
CO3	The student will learn to manipulate matrices and to do matrix algebra, determinants, eigen values Eigen vectors and to solve the system of linear equations.
CO4	The student will learn to understand how signals, systems, control.
CO5	The student will learn to understand how signals, systems, signal processing.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1	H				
	CO2		M			M
	CO3	H				
	CO4			M		
	CO5				L	
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I ONE DIMENSIONAL RANDOM VARIABLES 12

Random variables and their functions - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Exponential, Gamma, Weibull and Normal distributions.

UNIT II MATRIX THEORY 12

Eigen values using QR Transformations generalized eigenvectors – Canonical forms, singular valued composition and application – matrix norms and induced norms Psuedo inverse – least square approximations

UNIT III SPECIAL FUNCTIONS 12

Bessel's Equation- Bessel Functions- Legendre's Equation- Legendre Polynomials- Rodrigue's Formula- Recurrence Relations- Generating Functions and Orthogonal Property for Bessel Function of the First Kind.

UNIT IV OPERATIONS RESEARCH 12

Network Definitions – Minimal Spanning Tree algorithm – Shortest Route Problem – Maximal Flow model – Minimum Cost Capacitated Flow Problem – CPM and PERT.

UNIT V QUEUING THEORY 12

Single and Multiple Server Markovain Queuing Models – Customer Impatience Priority Queues M/g / I Queuing System –Queuing Applications.

TEXT BOOKS:

1. Handy A.Taha., "Operations Research An Introduction", 7th Edn. Pearson Education , Chennai-113. 2002.
2. Donald Gross and Carl M. Harris, "Fundamentals of Queuing Theory", 2nd Edn.
3. Wiley India Pvt Ltd, New Delhi.

REFERENCE BOOKS:

1. Freund J.D. and Miller JR "Probability Statistics for Engineers" Prentice Hall of India, 5th Edition, New Delhi. 1994.
2. Gupta.SC and Kapoor V.K. "Fundamentals of Mathematics Statistics" Sultan Chand & Sons, New Delhi.
3. Stewart G.W. "Introduction to Matrix Computaions" Academic Press, New York.

Course Code MVL101	**Course Name: SOLID STATE DEVICE MODELING AND SIMULATIONS**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Engineering Physics				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To apply all taught techniques to learn the modeling of bipolar devices and to understand about the modeling of MOSFET and to learn about the circuit simulators.

COURSE OUTCOMES (COs)

CO1	To Understand the complicated device models that are widely used in VLSI tools.
CO2	To Understand the changes introduced in the device models as well as contribute to the development of appropriate device models
CO3	To Understand the complicated MOSFET Modeling.
CO4	To Understand the complicated device models that is widely used in CAD tools.
CO5	To Understand the changes introduced in the device models as well as contribute

	to the development of appropriate EKV models					
Mapping of Course Outcomes with Program outcomes (POs) (H/M/L indicates strength of correlation) H-High, M-Medium, L-Low						
1	COs/Pos	a	b	c	d	E
2	CO1	H				
	CO2			L		L
	CO3		M			
	CO4	H			M	
	CO5		M			M
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I BASIC SEMICONDUCTOR PHYSICS **7**

Quantum Mechanical Concepts, Carrier Concentration, Transport Equation Bandgap, Mobility and Resistivity, Carrier Generation and Recombination Avalanche Process, Noise Sources.

UNIT II MODELING BIPOLAR DEVICE PHENOMENA **10**

Injection and Transport Model, Continuity Equation, Diode Small Signal and Large Signal (Charge Control Model), Transistor Models: Ebber – Molls and Gummel Poon Model, Mextram Model, Spice Modeling Temperature and Area Effects.

UNIT III MOSFET MODELING **10**

Introduction Inversion Layer, MOS Transistor Current, Threshold Voltage, Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE.

UNIT IV PARAMETER MEASUREMENT **10**

General Methods, Specific Bipolar Measurement, Depletion Capacitance, Series Resistances, Early Effect, Gummel Plots, MOSFET: Long and Short Channel Parameters, Statistical Modeling of Bipolar and MOS Transistor.

UNIT V OTHER MOSFET MODELS **9**

The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non-quasi-static modeling, Noise model, temperature effects, MOS model 9, MOSAI model, PSP model, Influence of process variation, Modeling of device mismatch for Analog/RF Applications.

TEXT BOOKS:

1. Philip E. Allen, Douglas R.Hoberg. "CMOS Analog Circuit Design" Second Edition, Oxford Press-2002 (Unit III)
2. CMOS/BICMOS CLSI Low Voltage Power Kiat Seng Yeo,Samir S Rofail,Wang-Ling Gob,Person Education low price edition– 2002(Unit IV)

REFERENCES BOOK:

1. S.M. Sze "Semiconductor Devices – Physics and Technology". John Wiley and Sons 1985 (Unit 1.Unit II)
2. Giuseppe Massobrio and Paolo Antogentti, "Semiconductor Device Modeling with SPICE "Second Edition, McGraw-Hill Inc, New York. 1993 (Unit I, Unit II and Unit III).
3. Mohammed Ismail & Tern Fiez "Analog VLSI – Signal & Information Processing",(Statistical Modeling of Mosfet unit IV).

Course Code MAE102	**Course Name: Advanced digital system design**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Digital communication				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To learn the concepts of theorems and other techniques to design minimized logic functions and To Understand the concepts of synchronous and asynchronous sequential circuit design and

COURSE OUTCOMES (COs)

CO1	Ability to analyze and design sequential digital circuits
CO2	Ability to understand the requirements and specifications of the system required for a given application
CO3	Ability to understand programmable logic devices
CO4	To learn about the faults in logic circuits and metods of diagnoising it
CO5	To learn about programmable logic devices.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		M			
	CO2	H				L
	CO3	H			M	
	CO4		M			M
	CO5			L		

3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I ADVANCED TOPICS IN BOOLEAN ALGEBRA **9**

Shannon's expansion theorem, Consensus theorem, Octal designation, Run measure, INHIBIT/INCLUSION/AOI/Driver /Buffer gates ,Gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method ,Design of static hazard free and dynamic hazard free logic circuits.

UNIT II STNCHRONOUS SEQUENTIAL CIRCUIT DESIGN **9**

Analysis of clocked synchronous sequential Networks (CSSN), Modeling of CSSN,State table assignment and reduction, Design of CSSN,Design of iterative circuit, ASM Chart, ASM Realization. Design of Arithmetic circuits for Fast adder,Array Multiplier.

UNIT III ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN **9**

Analysis of Asynchronous Sequential Circuit (ASC) ,Flow Table Reduction , Races in ASC , State Assignment Problem and the Transition Table, Design of ASC ,Data Synchronizers, Designing vending Machine Controller, Mixed Operating Mode Asynchronous Circuits.

UNIT IV FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS **9**

Fault Table Method ,Path Sensitization Method, Boolean Difference Method,Kohavi Algorithm, Tolerance Techniques , The Compact Algorithm,Practical PLA"s, Fault in PLA Circuit Test Approach, Transition Check Approach , State identification and fault detection experiment .

UNIT-V PROGRAMMMABLE LOGIC DEVICES **9**

Basic concepts, Programming technologies, Programmable Logic element(PLE),Programmable Logic Array(PLA),System Design using PLD's-Design of combinational and sequential circuits using PLD's(CPLD).Programming PAL device using PALSAM ,Design of state machine using Algorithmic State Machines (ASM) chart as a design tool, Introduction to Field Programmable Gate Arrays –Types of FPGA, Xilinx XC 3000 series, Logic Cell Array (LCA),Configurable Logic Blocks(CLB) INPUT/OUTPUT Block(IPB)-Programmable Interconnect Point (PIP),Introduction to Actel AACT2 FAMILY AND XILINX XC 4000 families ,Design examples.

TEXT BOOK:

1. William I.Flectcher, “An Engineering Approach to Digital Design”, PrenticeHall of India.
2. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
3. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
4. Digital Circuits and Logic Design – Samuel C. Lee , PHI

REFERENCES BOOK:

1. Donald G. Givone, “Digital principles and Design”, Tata McGraw Hill 2002.
2. Parag K Lala, “Digital System design using PLD”, BS Publications, 2003.
3. John M Yarbrough, “Digital Logic applications and Design”, Thomson Learning, 2001.
4. Nripendra N Biswas, “Logic Design Theory”, Prentice Hall of India, 2001.
5. Charles H. Roth Jr., “Fundamentals of Logic design”, Thomson Learning, 2004.

Course Code MVL102	**Course Name: INTRODUCTION TO VLSI DESIGN**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Basic VLSI Design				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To understand the concepts of MOS transistors operations and their AC , DC Characteristics and To know the fabrication process of CMOS technology and its layout design rules and To know the concepts of power estimation and delay calculations in cmos circuits

COURSE OUTCOMES (COs)

CO1	To learn the basic MOS and CMOS circuit, characteristics and performance.
CO2	To learn the circuit components at physical level design.
CO3	To learn the different abstract levels in Verilog for modeling digital circuits.
CO4	To learn about the VLSI circuit components and physical design
CO5	To study the concepts of Verilog in designing digital logic circuits.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H		M	
	CO2	L				L
	CO3			L		
	CO4		M			M
	CO5		H		M	
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)

			√			
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UNIT – I MOS TECHNOLOGY AND CIRCUITS **9**

MOS Technology and VLSI, Process parameters and consideration for BJT, MOS and CMOS, CMOS logic, MOS transistor theory , Enhancement mode transistor action, Ideal I-V characteristics, DC transfer characteristics, Threshold voltage, Body effect,Design equations, Second order effects. MOS models and small signal AC characteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance model

UNIT –II CMOS CIRCUITS DESIGN PROCESS **9**

CMOS fabrication, P -Well process, N -Well process, twin - tub process, MOS layers stick diagrams and Layout diagram, Layout design rules, Latch up in CMOS circuits, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION

9

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT – IV **VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN** 9

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits, Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modelling, cross talk, floor planning, power distribution ,Clock distribution.

UNIT V SPECIFICATION USING VERILOG HDL **9**

Basic concepts- identifiers- gate primitives, gate delays, operators, timing controls, procedural assignments conditional statements, Data flow and RTL, structural gate level switch level modeling, Design hierarchies, Behavioral and RTL modeling, Test benches, Design of decoder, equality detector, comparator, priority encoder, half adder, full adder, Ripple carry adder, D latch and D flip flop

TEXT BOOK:

1. Douglas A. Pucknell and Kamran Eshraghian, “Basic VLSI Design Systems and Circuits”, Prentice Hall of India Pvt. Ltd., 1993.
2. Wayne Wolf, ”Modern VLSI Design”, 2nd Edition, Prentice Hall 1998.
3. Amar Mukherjee, “Introduction to NMOS and CMOS VLSI System Design,” Prentice Hall,

REFERENCES BOOK:

1 . John P.Uyemura “Introduction to VLSI Circuits and Systems”, John Wiley & Sons, Inc.,2002..
2 Fabricious E. “Introduction to VLSI Design”, McGraw Hill, 1990.
3 J.Bhasker: Verilog HDL primer, BS publication,2001
4. Ciletti Advanced Digital Design with the Verilog HDL, Prentice Hall of India, 2003

Course Code MVLIL1	Course Name: VLSI DESIGN LAB I	L	T	P	C
	Total Contact Hours: 45	0	0	4	2
	Prerequisite: Digital VLSI CMOS				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To learn about the design of digital circuits using Hardware description languages

COURSE OUTCOMES (COs)

CO1	To learn about the design of digital circuits of HALF ADDER, FULL ADDER Hardware description languages
CO2	To learn about the design of digital circuits of HALF SRACTOR/FULL SUBTRACTOR
CO3	To learn about the design of digital circuits of MULTIPLEXER, DEMULTIPLEXER using Hardware description languages
CO4	To learn about the design of digital circuits of ENCODER, DECODER using Hardware description languages
CO5	To learn about the design of digital circuits of JK, D, T, SR FLIPFLOPS

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1			H		L
	CO2	M	H			
	CO3			M		M
	CO4		H		M	
	CO5		M			
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

LIST OF EXPERIMENTS

(ALL SHOULD BE DONE USING VERILOG HDL & VHDL CODE ON FPGA)

1. DESIGN AND TESTING OF HALF ADDER, FULL ADDER.
2. DESIGN AND TESTING OF HALF SRACTOR/FULL SUBTRACTOR.

3. DESIGN AND TESTING OF MULTIPLEXER, DEMULTIPLEXER.
4. DESIGN AND TESTING OF ENCODER, DECODER.
5. DESIGN AND TESTING OF MAGNITUDE COMPARATOR WITH 8 BITS.
6. DESIGN AND TESTING OF CODE CONVERTERS.
7. DESIGN AND TESTING OF JK, D, T, SR FLIPFLOPS.
8. DESIGN AND TESTING OF COUNTERS.
9. DESIGN AND TESTING OF UP/DOWN COUNTERS, RAM & ROM.
10. DESIGN AND TESTING OF N- BIT SHIFT REGISTERS.
11. DESIGN AND TESTING OF ALU.

Students will be able to design and implement digital logic circuits on FPGA

SEMESTER II

Course Code MAE201	**Course Name: Analysis and design of analog integrated circuits**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Linear Integration Circuits				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To design the single stage amplifiers using pmos and nmos driver circuits with different loads and analyse high frequency concepts of single stage amplifiers and noise characteristics associated v differential amplifiers

COURSE OUTCOMES (COs)

CO1	Ability to analyse the design of single and two stage operational amplifiers and voltage references, and determine the device dimensions of each MOSFETs involved.
CO2	To understand the design techniques of switched capacitor filters
CO3	To study the different types of current mirrors
CO4	To know the concepts of voltage and current reference circuits
CO5	To understand about MOS switched capacitor filters.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2		M			L
	CO3	H				
	CO4		M		M	

	CO5			L		M
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT-I CIRCUIT CONFIGURATION FOR LINEAR IC

9

Current source, analysis of difference amplifiers with active load, Supply and temperature independent biasing techniques, voltage references.

UNIT-II OPERATIONAL AMPLIFIERS

9

Analysis of operational amplifier circuits, slew rate model and high frequency analysis, operational amplifier noise analysis and low noise operational amplifiers.

UNIT-III ANALOG MULTIPLIER AND PLL

9

Analysis of MOS operational Amplifier, CMOS voltage references, MOS Power amplifier and analog switches.

UNIT-IV MOS ANALOG ICS

9

Design of MOS Operational Amplifier,CMOS Voltage references,MOS power amplifier and analog switches.

UNIT-V MOS SWITCHED CAPACITOR FILTERS

9

Design techniques for switched capacitor filter, CMOS switched capacitor filters, MOS integrated active RC filters.

TEXT BOOK:

1. Kenneth R.Laker, Willy M.C.Sansen, William M.C.Sansen, "Design of Analog Integrated Circuits and Systems ", McGraw Hill, 1994.
2. Behzad Razavi, "Principles of Data Conversion System Design", S.Chand &Company ltd, 2000.

REFERENCES BOOK:

1. Gray and Meyer, "Analysis and Design of Analog IC's, Wiley International, 1996.
2. Gray, Wooley, Broderson, "Analog MOS Integrated Circuits", IEEE Press 1989.

Course Code MVL201	**Course Name: COMPUTER AIDED DESIGN OF VLSI CIRCUITS**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Basic VLSI Design				

	Course Designed by : Dept. of Electronics And Communication Engineering

OBJECTIVES

To study various physical design methods in VLSI and To understand the concepts behind the VLSI design rules and routing techniques

COURSE OUTCOMES (COs)

CO1	To understand about algorithms and graph theory for the development of VLSI tools
CO2	To know the limitations and advantages of CAD tools by means of which they can be operated successfully**.**
CO3	To understand the concepts behind the VLSI design rules and routing techniques
CO4	To use the simulation techniques at various levels in VLSI design flow.
CO5	To understand the concepts of various algorithms used for floor planning placement and routing techniques

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2			M		L
	CO3		H			
	CO4	L				
	CO5				M	
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT – I INTRODUCTION TO VLSI **9**

Introduction to VLSI Methodologies – VLSI Physical Design Automation – Design and Fabrication of VLSI Devices – Fabrication Process and its impact on Physical Design.

UNIT – II DESIGN AUTOMATION TOOLS **9**

A Quick Tour of VLSI Design Automation Tools – Data Structures and Basic Algorithms – Algorithms Graph Theory and Computational Complexity – Tractable and Intractable Problems.

UNIT – III Methods for Optimization

9

General purpose methods for combinational optimization – partitioning – Floor Planning and Pin Assignment – Placement – Routing.

UNIT – IV SIMULATION

9

Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT – V HIGH LEVEL SYNTHESIS

9

High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

TEXT BOOK:

1. N.A Sherwani, "Algorithms for VLSI Physical Design Automation", 1999.

REFERENCES BOOK:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", 1998.

Course Code MVL202	**Course Name: LOW POWER VLSI DESIGN**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: VLSI Design				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To know the sources of power consumption in CMOS circuits and To understand the various power reduction techniques and the power estimation methods and

COURSE OUTCOMES (COs)

CO1	To know the basics and advanced techniques in low power
CO2	To design as reduction of power is much needed to enhance the performance of the system
CO3	To study the design concepts of High power circuits.
CO4	To understand the various power reduction techniques and the power estimation
CO5	To study the design concepts of low power circuits.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		M			
	CO2		H			L
	CO3	L				
	CO4			M		M

	CO5				L	
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I INTRODUCTION 9

Introduction – Simulation – Power Analysis – Probabilistic Power Analysis.

UNIT II ARCHITECTURE 9

Circuit – Logic – Special Techniques – Architecture and Systems.

UNIT III ADVANCED TECHNIQUES 9

Advanced Techniques – Low Power CMOS VLSI Design – Physical of Power Dissipation in CMOS FET Devices.

UNIT IV POWER ESTIMATION 9

Power Estimation – Synthesis for Low Power – Design and Test of Low Voltages – CMOS Circuits.

UNIT V LOW POWER ESTIMATION 9

Low Power Static RAM Architectuers – Low Energy Computing Using Energy Recovery Techniques – Software Design for Low Power.

Text Books:

1. **1.** Gary Yeap "Practical Low Power Digital VLSI Design", 1997.

References:

1. Kaushik'Roy, Sharat Prasad, "Low Power VLSI Circuit Design" 2000.

Course Code MVL2L2	**Course Name: VLSI DESIGN LAB II**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	0	0	4	2
	Prerequisite: VLSI Design lab I				
	Course Designed by : Dept. of Electronics And Communication Engineering				
OBJECTIVES: Physical design of CMOS logic can be known and SPICE simulation of analog circuits wii be carried out to measure its related parameters.					

COURSE OUTCOMES (COs)	
CO1	To understand about layout in VLSI design
CO2	To understand about SPICE simulation of basic analog citcuits.
CO3	To understand about placement and routing in VLSI design
CO4	To understand about SPICE simulation of basic Digital citcuits.
CO5	To understand about routing in VLSI design

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2		M			
	CO3	L	H			L
	CO4			H	L	
	CO5		M			
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

1. Introduction to layout design rules

Layout, physical verification, placement & route and static timing analysis for the following:

2. CMOS inverter

3.CMOS NOR/ NAND gates

4. CMOS XOR and MUX gates

5. CMOS half adder and full adder

6. Static / Dynamic logic circuits (register cell)

7. Latch

8. Pass transistor

9. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths

10. Introduction to SPICE simulation and coding of NMOS/CMOS circuit

11. SPICE simulation of basic analog circuits: Inverter / Differential amplifier

12. Analog Circuit simulation (AC analysis) – CS & CD amplifier

13. System level design using PLL

LIST OF ELECTIVES

Course Code MVL001	Course Name: CMOS VLSI DESIGN	L	T	P	C
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Basic CMOS VLSI Design				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To understand about the basic concepts of CMOS logic and To learn about the performance estimation of CMOS logic and To understand about the design strategies and CMOS subsystem design.

COURSE OUTCOMES (COs)

CO1	To understand about the basics of CMOS technology and its performance estimation.
CO2	To understand about the design strategies and CMOS design.
CO3	To understand about the basic concepts of CMOS logic
CO4	To learn about the performance estimation of CMOS logic
CO5	To learn about the design strategies used in Digital CMOS VLSI subsystem.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2	L				L
	CO3		H			
	CO4			M		
	CO5				L	
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I INTRODUCTION TO CMOS CIRCUITS 9

MOS Transistors, MOS Transistors switches, CMCS logic circuit and System representations, MOS Transistor theory – Introduction MOS device design equation, the

complementary CMOs inverter – DC characteristics, Static Load MOS inverters, The differential inverter, The transmission gate, The Tri state inverter, Bipolar Devices.

UNIT II CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION 9

Introduction, Resistance estimation, Capacitance estimation, Inductance estimation, Switching characteristics of CMOS gate Transistor, Sizing, Power Dissipation, Sizing Routing conductors, Charge sharing, Design Margining, Reliability.

UNIT III CMOS CIRCUIT AND LOGIC DESIGN 9

CMOs Logic Gate design, Basic Physical Design of simple gate, CMOS Logic structures clocking strategies, i/o Structures, Low Power Design.

UNIT IV SYSTEMS DESIGN AND DESIGN METHOD 9

Design Strategies CMOS chip Design options, Design Methods, Design Capture Tools, Design Verification Tools, Design Economics, and Data Sheets. CMOS Testing – Manufacturing Test Principles, Design Strategies for Test, Chip level Test Techniques, System Level Test Techniques, and Layout Design for Improved Testability.

UNIT V CMOS SUB SYSTEM DESIGN 9

Data path operations – Additions/Subtraction party generators, Comparators. Zero/one Detectors, Binary Counters, ALU's, Multiplication shifters, Memory Elements, Control-FSM, Control Logic Implementation.

TEXT BOOK:

1. Nell H E Weste and Kamran Eshraghian, "Principles Of CMOS VLSI Design", 2nd Edition, Addision Westley, 1998.

REFERENCES BOOK:

1. Jaycob Backer, Harry W L and David E Byce, "CMOS Circuit Design, Layout and Simulation", PHI, 1998.

Course Code MVL 002	**Course Name: VLSI SIGNAL PROCESSING**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Digital Signal Processing				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To understand the various VLSI architectures for digital signal processing and To know the techniques of critical path and algorithmic strength reduction in the filter structures and To study the performance parameters, viz. area, speed and power.

COURSE OUTCOMES (COs)

CO1	Ability to modify the existing or new DSP architectures suitable for VLSI
CO2	To know the techniques and algorithmic strength reduction in the filter structures
CO3	To understand the various VLSI architectures for digital signal processing
CO4	To study the performance parameters area.
CO5	To study the performance parameters speed and power

Mapping of Course Outcomes with Program outcomes (POs) (H/M/L indicates strength of correlation) H-High, M-Medium, L-Low						
1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2			M		M
	CO3		H			
	CO4	L			M	
	CO5		H			
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS 9

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm,Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION 9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 9

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TEXT BOOKS:

1. **1.** Keshab K. Parthi, "VLSI Digital Signal Processing Systems", Design and implementation, Wiley, Inter Science, 1999.
2. S.Y. Kung, H.J. White House, T.Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.

REFERENCE BOOK:

1. Jose E. France, Yannis Tsividis, "Design of Analog – Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.

Course Code MVL003	**Course Name: ANALOG VLSI DESIGN**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Basic VLSI Design				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To study the concepts of CMOS and BICMOS analog circuits and To understand the concepts of A/Dconvertors and analog integrated sensors and To understand the testing concepts in analog vlsi circuits and its statistical modelling.

COURSE OUTCOMES (COs)

CO1	To Understand that analog circuits are essential in interfacing and building amplifiers and low p filters.
CO2	To understand the concepts of A/D convertors and analog integrated sensors
CO3	To understand the concepts of CMOS and BICMOS analog circuits
CO4	To understand the testing concepts in analog vlsi circuits.
CO5	To understand the testing concepts in statistical modeling.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			

	CO2		H			
	CO3	L		M		M
	CO4		M		M	
	CO5	M		M		
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT-I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW VOLTAGE SIGNAL PROCESSING 9

Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques –Super MOS Transistor-Primitive Analog Cells-Linear Voltage-Current converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low BiCMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT-II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT-MODE SIGNAL MESSING AND NEURAL INFORMATION PROCESSING

9

Continuous-Time Signal Processing-Sampled-Data Signal Processing-artiched-current Data Converters-Practical Consideration in SI Circuits Logically-Inspired Neural Networks-Floating-Gate,Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-contrast Sensitive Silicon Retina

UNIT III SAMPALED-DATA ANALOG FILTERS,OVER SAMPLED A/D CONVERTERS AND ANALOG INTERGRATED SENSORS

9

First-order and second SC Circuits-Bilinear transformation-Cascade Design-Switched-Capacitor Ladder-Synthesis of Switched –Current filter-Nyquist rate A/D converters-Modulators for over Sampled A/D conversion- First and second Order and Multibit Sigma-Delta Modulators-interpolative Modulators-Cascade Architecture-Decimation Filters-Mechanical, Thermal, Humidity and Magnetic Sensors-Sensor interfaces.

UNIT IV DESIGN FOR TESTABLITY AND ANALOG VLSI INTERCONECTORS

9

Faults modeling and Simulation- Testability-Analysis Technique-AdHoc Methods and General Guidelines Scan Techniques-Boundary Scan-Built-in self Test- Analog Test Buses-Design for Election-Beam Testability-Physics of Interconnects in VLSI- Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping analog Circuits.

UNIT V STATISTICAL MODELLING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT 9

Review of statistical concepts- statistical Device Modeling-Statistical Circuit Simulation-Automation Analog Circuit Design-Automatic Analog Layout-CMOS Transistor layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog-Digital Layout.

TEXT BOOKS:

1. "Analog VLSI Signal and information Processing",Mohammed Ismail,Terri Fiez, McGraw-Hill International Editions,1994.

REFERENCE BOOK:

1. Malcom R. Haskard, Lan C. May, "Analog VLSI Design- NMOS and CMOS", Prentice hall,1998.
2. Randall I. Geiger, Phillip & Allen, Neol K. Strader, "VLSI Design Techiniques for Analog and Digital Circuits", McGraw Hill International Company,1990
3. Jose E. France, Yannis Tsividis, "Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing," Prentice Hall, 1994

Course Code MVL004	Course Name: **SYSTEM ON CHIP DESIGN**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Digital VLSI Design				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To learn System on chip fundamentals, their applications and to gain knowledge on NOC design and to le the various Computation models of SOCs.

COURSE OUTCOMES (COs)

CO1	To understand about IP cores and application specific design
CO2	To Understand About System Design With Model Of Computation And Co-Design
CO3	To learn the Computation–Communication Partitioning And Network On Chip-Based Soc
CO4	To gain knowledge on NOC design
CO5	To learn the various Computation models of SOCs.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1			M		
	CO2		H		L	
	CO3		H			
	CO4	L		M		M
	CO5					

3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I INTRODUCTION 9

Introduction to SoC Design., Platform-Based SoC Design., Multiprocessor SoC and Network on Chip, Low-Power SoC Design

UNIT II SYSTEM DESIGN WITH MODEL OF COMPUTATION AND CO-DESIGN 9

System Models, Validation and Verification, Hardware/Software Codesign Application Analysis, Synthesis.

UNIT III COMPUTATION–COMMUNICATION PARTITIONING AND NETWORK ON CHIP-BASED SOC 9

Communication System: Current Trend, Separation of Communication and Computation. Communication-Centric SoC Design, Communication Synthesis, Network-Based Design, Network on Chip, Architecture of NoC

UNIT IV NOC DESIGN

9 Practical Design of NoC, NoC Topology-Analysis Methodology, Energy Exploration, NoC Protocol Design, Low-Power Design for NoC: Low-Power Signaling, On-Chip Serialization, Low-Power Clocking, Low-Power Channel Coding, Low-Power Switch, Low-Power Network on Chip Protocol

UNIT V NOC /SOC CASE STUDIES

9 Real Chip Implementation-BONE Series-,BONE 1-4, Industrial Implementations-,Intel's Tera-FLOP 80-Core NoC, Intel's Scalable Communication Architecture, Academic Implementations-FAUST, RAW;design case study of SoC –digital camera

TEXT BOOK:

1. Hoi-jun yoo, Kangmin Lee, Jun Kyoung kim, "*Low power NoC for high performance SoC desing",*CRC press, 2008.

REFERENCES BOOK:

1. Vijay K. Madisetti Chonlameth Arpikanondt, *"A Platform-Centric Approach to System-on-Chip (SOC) Design",* Springer, 2005.

Course Code MVL005	Course Name: DESIGN OF SEMI CONDUCTOR MEMORIES	L	T	P	C
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Basic VLSI Design				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To study the architectures for SRAM and DRAM and To know about various non-volatile memories and To study the fault modelling and testing of memories for fault detection and To learn the radiation hardening process and issues for memory.

COURSE OUTCOMES (COs)

CO1	To know the design of MOS memories and the various precautionary methods to be used in their design.
CO2	To gain knowledge on various testing methods of semiconductor memories.
CO3	To get an overview on reliability of semiconductors.
CO4	To know about various non-volatile memories
CO5	To learn the radiation hardening process and issues for memory.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2		H			L
	CO3	L			L	
	CO4		M			
	CO5			M		
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I RANDOM ACESS MEMORY TECHNOLOGY **9**

Static Random Access Memories(SRAM) SRAM Cell Structure-MOS SRAM Architecture-MOS SRAM Cell and Peripherals Circuit Operation – Bipolar SRAM Technologies –Silicon On Insulator (Sol) Technology – Advanced SRAM Architecture and Technologies – Application Specific SRAMs Dynamic Random Access Memoirs(DRAMs) DRAM Technology Development – CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures-BICMOS DRAMs – Soft Error Failure in DRAMs – Advanced DRAM Designs and Architecture – Application Specific DRAMs.

UNIT II NON VOLATILE MEMORIES 9

Mask Read Only Memories(ROMs)-High Density ROMs-Programmable Read Only Memories(PROMs)-Bipolar PROMs CMOS PROMs-Erasable (UV) – Programmable Read Only Memories(EPROMs) - Floating – Gate EPROM Cell-One Time Programmable (OTP) EPROMs -Electrically Erasable PROMs(EEPROMs) – EEPROM Technology and Architecture – Non Volatile SRAM – Flash Memories (EPROM or EEPROM)

UNIT III MEMORY FAULTS MODELLING, TESTING AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE 9 RAM Fault, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault modeling and Testing-Application Specific Memory Testing

UNIT IV SEMICONDUCTOR MEMORY RELIABILITY AND RANDOM EFFECTS 9

General Reliability Issues-RAM Failure Modes and Mechanism - Nonvolatile Memory Reliability – Reliability Modeling and Failure Rate Prediction – Design for Reliability – Reliability Test Structures – Reliability Screening and Qualification. Radiation Effects-Single Event Phenomenon (SEP) – Radiation Hardened Memory Characteristics – Radiation Hardness Assurance and Testing – Radiation Dosimettry - Water Level Radiation Testing and Test Structures.

UNIT V ADVANCED MEMORY TECHNOLOGIES AND HIGH DENSITY MEMORY PACKAGING TECHNOLOGICS 9 Ferroelectric Random Access Memories (FRAMs) – Gallium Arsenide (GaAs) FRAM – Analog Memories Magneto Resistive Ferroelectric Random Access Memories (MRAMS) – Experimental Memory Devices Memory Hybrids and MCMs (2D – Memory Stacks and MCMs 3D) – Memory MCM Testing and Reliability Issues – Memory Cards – High Density Memory Packing Feature Directions.

TEXT BOOKS:

1.Ashok K. Sharma, “Semiconductor Memories Technology, Testing, and Reliability”, Prentice Hall of India Limited. New Delhi 1997.

REFERENCES BOOK:

1. Gray and Meyer, “Analysis and Design of Analog IC‘s, Wiley International, 1996.

Course Code MVL006	Course Name: VLSI ARCHITECTURE AND DESIGN METHODOLOGIES	L	T	P	C

	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Computer Design Methodologies				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To understand about the advanced topics in Boolean algebra and To know about analog and high speed VLSI and To know in detail about programmable ASICs and its interconnects and To understand about simulation and testing of VLSI circuits.

COURSE OUTCOMES (COs)

CO1	To understand about programmable ASIC its logic synthesis, simulation and testing of VLSI circuits
CO2	To know in detail about programmable ASICs and its interconnects
CO3	To know about analog and high speed VLSI
CO4	To understand about Programmable Asic Design Software
CO5	To understand about simulation and testing of VLSI circuits.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2	L		M		
	CO3				L	
	CO4		H			L
	CO5		M			
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT – I INTRODUCTION 9

Overview of a Digital VLSI design Methodologies- Trends in IC Technology advanced Boolean algebra- Shannon's expansion theorem- consensus theorem – Octal designation-Run Measure – Buffer gates- Gate Expander- Reed Muller expansion- Synthesis of multiple output combinational logic circuits by product map method- Design of Static hazard free and dynamic hazard free logic circuits.

UNIT – II ANALOG VLSI AND HIGH SPEED VLSI **9**

Introduction to analog VLSI- Realisation of Neural Networks and switched capacitors filters- sub- micron Technology and GaAS VLSI technology.

UNIT – III PROGRAMMABLE ASICS **9**

Antifuse- Static RAM-EPROM and EEPROM technology – PREP bench marks – Actel ACT – Xilinx LCA- Altera FLEX- Altera MAX DC & AC inputs and outputs – clocks and power inputs – Xilinx I/O blocks.

UNIT – IV PROGRAMMABLE ASIC DESIGN SOFTWARE **9**

Actel ACT – Xilinx LCA- Xilinx EPLD - Altera MAX 5000 & 7000 – Altera Max 9000 – Design Systems – Logic synthesis – half gate ASIC – Schmatic entry – low level design language – PLA tools – EDIF – CFI design representation.

UNIT – V LOGIC SYNTHESIS , SIMULATION AND TESTING

Basic features of VHDL language for behavioral modeling and simulation – Summary of VHDL data types – Dataflow and structural modeling – VHDL and logic Synthesis – types of simulation – Boundary scan Test – fault Simulation – Automatic test Pattern Generation.

TEXTBOOK:

1. Willam I. Fletcher " An Engineering Approach to Digital Design" Prentice Hall of India 1996.
2. Amar Mukherjee, Introduction to NMOS and CMOS VLSI System Design. Prentice Hall of India 1986

REFERENCES BOOK:

1.M.J.S. Smith " Application – Specific Integrates Circuits ", Addison Wesley Longman Inc. 1997.

2.Fedrick J. Hill and Gerald R. Peterson. " Computer Aider Logical Design with emphasis on VLSI".

Course Code MVL007	Course Name: **SUBMICRON VLSI DESIGN**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: VLSI Design				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To introduce the Concepts of silicon realization of ASIC and Cmos devices at deep Submicron Level and To study and apply the deep Submicron concepts to Cmos low power devices and To study and discuss about Rf Cmos transistor sizing and its limitations.

COURSE OUTCOMES (COs)

CO1	To understand about the design constraints for CMOS devices at deep submicron level for low power
CO2	To understand about the reliability constraints while designing CMOS devices at submicron level.
CO3	To understand about the design constraints for CMOS devices at deep submicron level high speed
CO4	To study and apply the deep Submicron concepts to Cmos low power devices
CO5	To study and discuss about RF CMOS transistor sizing and its limitations.

Mapping of Course Outcomes with Program outcomes (POs) (H/M/L indicates strength of correlation) H-High, M-Medium, L-Low						
1	COs/Pos	a	b	c	d	E
2	CO1		M			
	CO2		H		M	L
	CO3	M		L		
	CO4		H			M
	CO5			M		
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I SILICON REALIZATION OF ASIC

9

Introduction-Handcrafted layout implementation-bit-slice layout implementation-Cell based layout implementation- gate array layout implementation-Hierchial design approach- The choice of layout implementation form

UNIT II LOW POWER DESIGN

9

-Sources of CMOS power consumption-technology options for low power-reduction of P-leak by technological measures Reduction of P-dyn by technology measures-reduction of P-dyn by reduced voltage process-design option for low power-computing power vs chip power-a scaling perspectives.

UNIT III DESIGN FOR RELIABILITY

9

Introduction-latch up in CMOS circuits-Electrostatics discharge-and its protection-Electro migration-Hot carrier degradation design for signal integrity-clock distribution and critical timing issues-clock generation and synchronization in different domain on a chip-the influence of interconnection-design organization

UNIT IV DEEP SUB MICRON

9

-RF CMOS Transistor downsizing limitations-. RF basic blocks layout implementation Submicron technology and layout dependent effects-input output interfacing, the bonding pad, the pad ring, electrostatic discharge prevention.

UNIT V CMOS DEVICES

9

Clamp CMOS devices, zener diode-input structure-output structure-pull up-pull down-i/o pad,power clamp-core/pad limitation I/O Pad description using Ibis-Connecting to the package-Signal propagation between integrated circuits

TEXTBOOK:

1. Deep-Submicron Cmos Ics: From Basics to Asics By Harry J. M. Veendrick
2. Low Power Design in Deep Submicron Electronics by W. Nebel, Jean P. Mermet

REFERENCES BOOK:

1. Low-Power Deep Sub-Micron CMOS Logic: Sub-threshold Current Reduction by P.R.Van Der Meer, Arie van Staveren, Arthur H. M. van Roermund

Course Code MVL008	**Course Name: TESTING OF VLSI CIRCUITS**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: VLSI Testing				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To know the various types of faults and also to study about fault detection, dominance and To know the concepts of the test generation methods-DFT-BIST.
To understand the fault diagnosis methods.

COURSE OUTCOMES (COs)

CO1	To familiarize with the principles used in the construction VLSI Design For Test (DFT) tools.
CO2	To develop more efficient tools from the fault coverage and speed point of view.
CO3	To study about fault detection and dominance
CO4	To know the concepts of the test generation methods-DFT-BIST.
CO5	To understand the fault diagnosis methods

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2		M			
	CO3		M		M	
	CO4		H			M
	CO5	M		L		

3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I TESTING AND FAULT MODELLING

9

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models– Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation

UNIT II TEST GENERATION

9

Test generation for combinational logic circuits – Testable combinational logic circuit design– Test generation for sequential circuits – design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY

9

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design – system level DFT approaches.

UNIT IV SELF – TEST AND TEST ALGORITHMS

9

Built-In self Test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS

9

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.

TEXT BOOK:

1. Viswani D. Agarval, Michael L. Bushnell, "Essential of Electronic Testing for Digital Memory & Mixed Signal VLSI Circuit". Kulwer Academic Publications, 1999.
2. Alfred L. Crounch "Design for Test for Digital IC's and Embedded Core Systems". – PHI 1999.
3. M.Abramovici, M.A.Breuer and A.D. Friedman, "Digital systems and Testable Design", Jaico Publishing House,2002.

REFERENCES BOOK:

1. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
2. M.L.Bushnell and V.D.Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002.

Course Code MVL009	Course Name: NANOSCALE DEVICES AND CIRCUIT	L	T	P	C
	Total Contact Hours: 45	3	0	0	3

	Prerequisite: Nano Techonology
	Course Designed by : Dept. of Electronics And Communication Engineering

OBJECTIVES

To learn about leakage current and its control and reduction techniques in CMOS devices and To know the device technologies for sub 100nm CMOS and To study the device scaling of single and multigate MOSFETs

COURSE OUTCOMES (COs)

CO1	To understand about the concepts of nanoscale devices which in turn can be used for high speed VLSI circuits.
CO2	To study the device scaling of single and multigate MOSFETs
CO3	To familiarize the low power design and voltage scaling issues in Nano scale devices
CO4	To study about various nanoscale devices
CO5	To design CMOS circuit using non-classical devices

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1			M		
	CO2		H			
	CO3		L			M
	CO4	L		H		
	CO5		M			
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I CMOS SCALING CHALLENGES IN NANOSCALE REGIMES 9

Leakage current mechanisms in nanoscale CMOS, leakage control and reduction techniques, process variations in devices and interconnects. Device technologies for sub 100nm CMOS: Silicidation and Cu-low k interconnects, strain silicon – biaxial stain and process induced strain; Metal-high k gate; Emerging CMOS technologies at 32nm scale and beyond – FINFETs, surround gate nanowire MOSFETs, heterostructure (III-V) and Si-Ge MOSFETs.

UNIT II DEVICE SCALING AND BALLISTIC MOSFET

9

Two dimensional scaling theory of single and multigate MOSFETs, generalized scale length, quantum confinement and tunneling in MOSFTEs, velocity saturation, carrier back scattering and injection velocity effects, scattering theory of MOSFETs.

UNIT III EMERGING NANOSCALE DEVICES

9

Si and hetero-structure nanowire MOSFETs, carbon nanotube MOSFETs, quantum wells, quantum wires and quantum dots; Single electron transistors, resonant tunneling devices.

UNIT IV NANOSCALE CMOS DESIGN

9

CMOS logic power and performance, voltage scaling issues; Introduction to low power design; Performance optimization for data paths.

UNIT V NANOSCALE CIRCUITS

9

Statistical circuit design, variability reduction, design for manufacturing and design optimization; Sequential logic circuits, registers, timing and clock distribution, IO circuits and memory design and trends. Non-classical CMOS: CMOS circuit design using non-classical devices – FINFETs, nanowire, carbon nanotubes and tunnel devices.

TEXT BOOK:

1. Lundstrom, M., "Nanoscale Transport: Device Physics, Modeling, and Simulation",Springer. 2000
2. Maiti, C.K., Chattopadhyay, S. and Bera, L.K., "Strained-Si and Hetrostructure Field Effect Devices", Taylor and Francis, 2007
3. Hanson, G.W., "Fundamentals of Nanoelectronics", Pearson, India., 2008.

REFERENCES BOOK:

1. Wong, B.P., Mittal, A., Cao Y. and Starr, G., "Nano-CMOS Circuit and Physical Design", Wiley, 2004
2. Lavagno, L., Scheffer, L. and Martin, G., "EDA for IC Implementation Circuit Design and Process Technology", Taylor and Francis, 2005

Course Code MAE101	**Course Name: ADVANCED DIGITAL SIGNAL PROCESSING**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Digital Signal Processing				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To introduce the Concepts of silicon realization of ASIC and Cmos devices at deep Level To study and apply the deep Submicron concepts to Cmos low power devices

COURSE OUTCOMES (COs)

CO1	To learn about random signal processing
CO2	To know about spectrum and linear estimation.
CO3	To know about adaptive filters
CO4	To understand the concepts related to Adaptive Filters

CO5	To understand the concepts related to multirate digital signal processing					
Mapping of Course Outcomes with Program outcomes (POs) (H/M/L indicates strength of correlation) H-High, M-Medium, L-Low						
1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2	M				
	CO3		H			
	CO4			M		
	CO5					H
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT-1 DISCRETE RANDOM SIGNAL PROCESSING

9

Discrete Random Processes,Expectations,Variance,Co-variance,Scalar product, Energy of Discrete Signals-Parseval's Theorem, Wiener Khintchine Relation-Power Spectral Density-Periodogram-Sample Autocorrelation-Sum Decomposition Theorem, Spectral Factorization Theorem-Discrete Random Signal Processing by Linear Systems-Simulation of White Noise-Low Pass filtering of white noise.

UNIT-II SPECTRUM ESTIMATION

9

Non-Parametric Methods–Correlation Method–Co-Variance Estimator-Performance Analysis of Estimator-Barlett Spectrum Estimation –Welch Estimation-Model Based Approach-AR,MA,ARMA Signal Modeling –Parameter Estimation using Yule-Walker Method.

UNIT-III LINEAR ESTIMATION AND PREDICTION

9

Maximum likelihood criterion-efficiency of estimator-least mean squared error criterion-Wiener filter –Discrete Wiener Hoff Equation–Recursive estimators–Kalman filter–linear prediction, prediction error whitening filter, inverse filter-Levinson recursion, Lattice realization and Levinson recursion algorithm for solving Toeplitz system of equations.

UNIT-IV ADAPTIVE FILTERS

9

FIR adaptive filters-Newton's steepest descent method-adaptive filter based on steepest descent method-Widrow Hoff LMS adaptive algorithm-Adaptive channel equalization-

Adaptive echocarcellor-Adaptive noise cancellation –RLS adaptive filter-Exponentially weighted RLS –Sliding window RLS –Simplified IIRLMS adaptive filter.

UNIT-V MULTIRATE DIGITAL SIGNAL PROCESSING 9

Mathematical description of sample rate-interpolation and Decimation-continuous time model direct digital approach-Decimation by an integer factor–interpolation by an integer factor-Single and multistage realization-poly phase realization-Application to Sub band coding-Wavelet transform and filter bank implementation of wavelet expansion of signals.

TEXTBOOKS:

1. Monson.H.Hayes, Statiscal Digital Processing and Modelling, John Wiley and Sons.INC, New York.1996.

REFERENCES BOOK:

1. Sophocles J.Orfanidis, OptimumSignal Processing, McGraw Hill.1990.
2. John.G.Proakis, Dimitris G.Manofakis.Digital Signal Processing Prentice Hall of India, 1995.

Course Code MAE004	**Course Name: ELECTROMATIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Testing of VLSI Circuits				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

EMI Environment and EMI Coupling Principles and EMI Specification, Standards and Limits and EMI Measurements and Control Techniques and EMC Design of PCBs.

COURSE OUTCOMES (COs)

CO1	Ability to analyze Electromagnetic interference effects in PCBs
CO2	Ability to propose solutions for minimizing EMI in PCBs
CO3	To understand UMI Test instruments/systems,EMI Test
CO4	To understand the EMI Control Techniques
CO5	To understand the EMC Design of PCBs

Mapping of Course Outcomes with Program outcomes (POs)

(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1			M		
	CO2				L	
	CO3		H			
	CO4		M			M
	CO5	L				

3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT-I EMI ENVIRONMENT/SPECIFICATIONS /STANDARDS

10

Sources of EMI conducted and radiated EMI, Transient EMI, EMI-EMC Definitions and units of parameters, unit of specifications, Civilian standards, and Military standards.

UNIT-II EMI COUPLING PRINCIPLES

10

Conducted, Radiated and Transient Coupling, common impedance ground coupling, radiated common mode and ground loop coupling radiated differential mode coupling, near field, cable to cable coupling, power mains and power supply coupling.

UNIT-III MEASUREMENTS

8

UMI Test instruments/systems,EMI Test ,EMI Shielded Chamber ,Open Area Test Site ,TEM Cell Antennas ,Conductors Sensors /Injectors /Couplers ,Military Test Method AND Procedures ,Calibration procedures.

UNIT-IV EMI CONTROL TECHNIQUES

8

Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, signal Control, Component Selection and mounting.

UNIT-V EMC DESIGN OF PCBS

9

PCB Traces Cross Talk, Impedance Control, Power Distribution decoupling, Zoning, Motherboard Designs and propagation Delay performance models.

TEXT BOOKS:

1. Bernhard Kerser, "Principles of Electromagnetic Compatibility", Artech house, 3rd Ed 1986.
2. Henry W.Ott, "Noise Reduction Techniques in Electronic Systems", John Wiley and Sons, New York, 1986.

REFERENCE BOOKS:

1. V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, 1986.

Course Code MVL010	**Course Name: OPTIMIZATION TECHNIQUES IN VLSI DESIGN**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3

	Prerequisite: Basic VLSI Design
	Course Designed by : Dept. of Electronics And Communication Engineering

OBJECTIVES

To Know in detail about the optimization techniques and to gain knowledge on Genetic algorithms and To learn implementation of genetic algorithms for VLSI physical design problems and To understand implementation of genetic algorithms for testing of VLSI circuits and technology mapping.

COURSE OUTCOMES (COs)

CO1	To Know in detail about the Statistical Modeling
CO2	To learn implementation of genetic algorithms for VLSI physical design problems
CO3	To Know in detail about the optimization techniques
CO4	To understand implementation of genetic algorithms for testing of VLSI circuits
CO5	To understand implementation of genetic algorithms for technology mapping

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2	M				
	CO3		H			L
	CO4				H	
	CO5			M		
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I STATISTICAL MODELING **9**

Modeling sources of variations, Monte Carlo techniques, Process variation modeling-Pelgrom‟s model, Principal component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models

UNIT II STATISTICAL PERFORMANCE, POWER AND YIELD ANALYSIS

9 Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level

statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation

UNIT III CONVEX OPTIMIZATION

9

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.

UNIT IV GENETIC ALGORITHM

9

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement,routing technology,Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multiway Partitioning Hybrid genetic-encoding-local improvement-WDFRComparison of Cas-Standard cell placement-GASP algorithm-unified algorithm.

UNIT V GA ROUTING PROCEDURES AND POWER ESTIMATION

9

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures.Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.

TEXT BOOKS:

1. Ashish Srivastava, Dennis Sylvester, David Blaauw "Statistical Analysis and Optimization for VLSI:Timing and Power" , Springer, 2005.

2. Pinaki Mazumder, E.Mrudnick, "Genetic Algorithm for VLSI Design,Layout and test Automation", Prentice Hall,1998

REFERENCES BOOK:

1. Stephen Boyd, Lieven Vandenberghe "Convex Optimization", Cambridge University

Course Code MVL011	**Course Name: VLSI FOR WIRELESS COMMUNICATION**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Wireless communication				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

- To study the design concepts of low noise amplifiers and to study the various types of mixers designed for wireless communication and to study and design PLL and VCO.

COURSE OUTCOMES (COs)

CO1	To know the concepts related to wireless communication in VLSI which can be efficiently implemented in real time**.**
CO2	To study the design concepts of low noise amplifiers.
CO3	To study the various types of mixers designed for wireless communication.
CO4	To study and design PLL and VCO.
CO5	To understand the concepts of CDMA in wireless communication.

Mapping of Course Outcomes with Program outcomes (POs) (H/M/L indicates strength of correlation) H-High, M-Medium, L-Low						
1	COs/Pos	a	b	c	d	E
2	CO1			H		
	CO2	M				
	CO3		M		M	
	CO4		H			L
	CO5				H	
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT I COMPONENTS AND DEVICES **9**

Integrated inductors, resistors, MOSFET and BJT AMPLIFIER DESIGN: Low Noise Amplifier Design - Wideband LNA - Design Narrowband LNA - Impedance Matching - Automatic Gain Control Amplifiers – Power Amplifiers

UNIT II MIXERS **9**

Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion - Low Frequency Case: Analysis of Gilbert Mixer – Distortion - High-Frequency Case – Noise- A Complete Active Mixer. Switching Mixer - Distortion in Unbalanced Switching Mixer - Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

UNIT III FREQUENCY SYNTHESIZERS **9**

Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector – Analog Phase Detectors – Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application).

UNIT IV SUB SYSTEMS **9**

Data converters in communications, adaptive Filters, equalizers and transceivers

UNIT V IMPLEMENTATIONS
9

VLSI architecture for Multitier Wireless System - Hardware Design Issues for a Next generation CDMA System .

Text Book:

1. B.Razavi ,"RF Microelectronics" , Prentice-Hall 1998.
2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002.
3. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', Cambridge University Press ,2003.

REFERENCES :

1. Emad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI Wireless Design - Circuits and Systems", Kluwer Academic Publishers, 2000.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 1999.
3. J. Crols and M. Steyaert, "CMOS Wireless Transceiver Design," Boston, Kluwer Academic Pub., 1997.

Course Code MAE202	**Course Name: COMPUTER ARCHITECTURE AND –PARALLEL PROCESSING**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Computer Architecture				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To understand the difference between the pipeline and parallel concepts and To study the various types of architectures and the importance of scalable architectures and To study the various memories and optimization of memory.

COURSE OUTCOMES (COs)

CO1	At the end of the course, the student will be able to:
CO2	Compare and evaluate the performance of various architectures.
CO3	Design sub-systems to meet specific performance requirements
CO4	Analyze the requirements of large systems to select and build the right infrastructure.
CO5	To study the various memories and optimization of memory.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		H			
	CO2			M		M
	CO3	M	H			
	CO4		M		M	
	CO5		H			

3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT-I THEORY OF PARALLESISM –PART-I

7

Parallel computer models-the state of computing, Multiprocessor and Multicomputer and Multivectors and SIMD computers, PRAM and VLSI mode Architectural development tracks .Program and properties Conditions of parallelism.

UNIT-II THEORY OF PARALLELISM –PART-II

10

Program partitioning and scheduling, Program flow mechanism, System inter connect architecture, Principles of scalable performance–performance matrices and measures, Parallel processing application speedup performance laws, scalability analysis and approaches.

UNIT-III HARDWARE TECHNOLOGIES

10

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory-backplane bus systems, cache memory organizations, shared memory organization, sequential and weal consistency model.

UNIT-IV PIPELINING AND SUPERSCALAR TECHNOLOGIES

10

Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivectors and SSIMD Computers, Scalable Multithread and dataflow architectures.

UNIT-V SOFTWARE AND PARALLEL PROCESSING

10

Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

TEXT BOOK:

1. Kai Hawang, “Advanced Computer Architecture”, McGraw Hill international, 1993.

REFERENCES BOOK:

1.William Stallings, “Computer Organization and Architecture”, Macmillan Publishing Company, 1990.

2. M.J.Quinn, “Designing Efficient Algorithms for Parallel Computer”, McGraw Hill International1994.

Course Code MED008	Course Name: REAL TIME OPERATING SYSTEMS	L	T	P	C
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Operating Systems				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

The aim of the course is to impart the concepts related to operating systems concepts and to discuss about RTOS application domains.

COURSE OUTCOMES (COs)

CO1	To understand about Operating system concepts
CO2	To know about various application domains in RTOS.
CO3	
CO4	
CO5	

Mapping of Course Outcomes with Program outcomes (POs)

(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1		M			L
	CO2	H			H	
	CO3			M		
	CO4		H			M
	CO5			M		
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT – I REVIEW OF OPERATING SYSTEMS **9**

Basic Principles – System calls – Files – Processes – Design and Implementation of Processes – Communication between Processes – Operating System Structures.

UNIT – II DISTRIBUTED OPERATING SYTEMS **9** Topology – Network types – communication – RPC- client server model- distributed file systems- design strategies.

UNIT – III REAL TIME MODELS AND LANGUAGES **9**

Events based – process based and graph based models – petrinet models – real time languages – RTOS tasks – RT scheduling – interrupt processing – synchronization control blocks – memory requirements.

UNIT – IV REAL TIME KERNEL **9**

Principles – design issues – Polled loop systems - RTOS porting to a target – comparison and study of various RTOS like QNX-VX works – PSOS – C executive - Case studies.

UNIT – V RTOS APPLICATION DOMAINS **9**

RTOS for image processing - Embedded RTOS for voice over IP – RTOS for voice over IP – RTOS for fault tolerant applications – RTOS for control systems.

Text Book:

1. Herma K, " Real time systems – Design for distributed Embedded Applications ", Kluwer Academic, 1997.
2. Charles Crowly, "Operating System – A design oriented approach" McGraw Hill, 1997.

References

1. R.J.A Bhur, D.L. Bailey, "An introduction to Real Time Systems', PHI 1999.
2. C.M. Krishna, Kang G Shin, "Real time systems", McGraw Hill, 1997

Course Code MED102	**Course Name: EMBEDDED SYSTEMS**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Microprocessor and its Application				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To know about the concepts of embedded hardware and to know in detail about PIC microcontroller.

COURSE OUTCOMES (COs)

CO1	To understand about the basics of embedded system and its software environment
CO2	To design embedded system for real time applications.
CO3	To know in detail about embedded microcontroller.
CO4	To discuss about the software environment in embedded systems.
CO5	To learn about real time operating systems.

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1			H		
	CO2				H	
	CO3		L			
	CO4			M		

	CO5				M	
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			
4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016				

UNIT – I INTRODUCTION REVIEW OF EMBEDDED HARDWARE

9

Terminology Gates – Timing Diagram – Memory – Microprocessors Busses – Direct Memory Access – Interrupts – Built – Ins on the Microprocessor – Conventions used on Schematic – Interrupt Microprocessor Architecture – Shared Data Problem – Interrupt Latency.

UNIT – II PIC MICROCONTROLLER AND INTERFACING

9

Introduction – CPU Architecture – Registers – Instruction Sets Addressing Modes – Loop Timers - Interrupts – Interrupt Timing I/O Expansion – 12C Bus Operation Serial EEPROM – Analog to Digital Converter – UART Baud Rate – Data Handling – Initialization – Special Features – Serial Programming – Parallel Slave Port.

UNIT – III EMBEDDED MICROCONTROLLER SYSTEMS

9

Motorola MC68H11 Family Architecture Registers - Addressing Modes – Programs – Interfacing Methods – Parallel I/O Interface – Parallel Port Interface – Memory Interfacing – High Speed I/O Interfacing - Interrupts – Interrupt SERVICE Routing – Features of Interrupts – Interrupt Vector and Priority – Timing Generation and Measurement – Input Capture – Output Compare – Frequency Measurement – Serial I/O Devices RS232, RS485 – Analog Interfacing – Applications.

UNIT – IV SOFTWARE DEVELAPMENT AND TOOLS

9

Embedded System Evolution Trends – Round – Robin with Interrupts – Function –One – Scheduling Architecture – Algorithms – Introduction to Assembler – Compiler – Cross Compilers and Integrated Development Environment (IDE) – Object Oriented Interfacing – Recursion – Debugging Strategies – Simulators.

UNIT –V REAL TIME OPERATING SYSTEMS

9

Task and Task States – Tasks and Data – Semaphores and Shared Data Operating System Services – Message Queues – Timer Function – Events – Memory Management – Interrupt Routines in an RTOS Environment – Basic Design Using RTOS.

TEXT BOOKS:

1. David E. Simon, "An embedded Software Primer" Pearson Education Asia, 2001.
2. John B Peat man "Design with Microcontroller" Pearson Education Asia, 1998.
3. Jonathan W. Volcano Brooks/Cole "Embedded Micro Computer Systems. Real Time Interfacing". Thomson Learning 2001.

REFERENCES BOOK:

1. Burns, Alan and Welling, Andy, "Real - Time Systems and Programming Languages", Second Edition, Harlow: Addison – Wesley – Longman, 1997
2. Raymond J. A. Blur and Donald L. Bailey, "Introduction to Real Time Systems: Design to Networking with C/C++" Prentice Hall Inc. New Jersey, 1999
3. Graham Moore, and Cylix, "Real – Time Programming: A Guide to 32 Bit Embedded Development. Reading" Addison - Wesley – Longman, 1998.

Course Code MED201	**Course Name: ASIC DESIGN**	**L**	**T**	**P**	**C**
	Total Contact Hours: 45	3	0	0	3
	Prerequisite: Basic ASIC				
	Course Designed by : Dept. of Electronics And Communication Engineering				

OBJECTIVES

To learn the fundamentals of ASIC and its design methods

COURSE OUTCOMES (COs)

CO1	To gain knowledge about partitioning
CO2	To analyses the synthesis
CO3	To gain knowledge on programmable architectures for ASICs
CO4	To understand the physical design of ASIC.
CO5	To understand the Asics Construction, Floor Planning, Placement And Routing

Mapping of Course Outcomes with Program outcomes (POs)
(H/M/L indicates strength of correlation) H-High, M-Medium, L-Low

1	COs/Pos	a	b	c	d	E
2	CO1			H		
	CO2			M		
	CO3	M			L	
	CO4		M			M
	CO5			M		
3	Category	Professional Mathematics (PM)	Professional Core (PC)	Professional Elective (PE)	Open Elective (OE)	Project/ Term Paper Seminar/ Internship (PR)
			√			

4	Approval	37th , 38th & 39th Meeting of Academic Council, May 2015, Jan 2016 & April 2016

UNIT – I INTRODUCTION TO ASIC, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Capacitance – Logical Effort – Library Cell Design – Library Architecture Types of ASIC **–** Design Flow – CMOS Transistors – CMOS Design Rules – Combinational Logic Cell – Sequential Logic Cell – Data Path Logic Cell – Transistors as Resistors – Transistor Parasitic**.**

UNIT –II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS. 9

Ant fuse – Static RAM – EPROM and EEPROM Technology – PREP Bench Marks – Acted ACT – Xilinx LCA – Altars FLEX – Alters MAX – DC & AC Input and Output – Clock and Power Input – Xilinx I/O Blocks.

UNIT – III PROGRAMMABLE ASICS INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY.

9

Acted ACT - Xilinx LCA - Xilinx EPLD - Alters MAX 5000 & 7000 - Alters MAX 9000 - Alters FLEX – Design System – Logic Synthesis – Half Gate ASIC – Schematic Entry – Low Level Design Language – PLA Tools – EDIF – CFI Design Representation**.**

UNIT – IV LOGIC SYNTHESIS, SIMULATION AND TESTING

9

Verilog and Logic Synthesis– VHDL and LOGIC Synthesis– Types of Simulation – Boundary Scan Test– Fault Simulation- Automatic Test Pattern Generation.

UNIT – V ASICS CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING.

9

System Partition – FPGA Partitioning – Partitioning Methods – Floor Planning – Placement – Physical Design Flow – Global Routing – Detailed Routing – Special Routing –Circuit Extraction – DRC.

TEXT BOOK:

1. M. J. S. Smith, “Application Specific Integrated Circuits” , Addison – Wesley L Ongnam Inc., 1997.

REFERENCE BOOK:

1. Andrew Brown, “VLSI Circuits and Systems in Silicon”, McGraw Hill 1991.
2. S. D. Brown, R. J. Francis, J. ROX, Z. G. Urines, “Field Programmable Publishers, 1992.
3. Mohammed Ismail and Terri Fief, “Analog VLSI and Modern Signal Processing,” McGraw Hill 1994.
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