Bharath Institute of Higher Education and Research

[Declared Under Section 3 of UGC Act, 1956]
Chennai – 600 073

INTERNAL QUALITY ASSURANCE CELL (IQAC)

DOCUMENTS SUBMISSION FORM

Date of Submission	24/08/2019
Type of Documents	Seminar-2019
Description	Seminar on **"VERIFICATION TRENDS FOR VLSI DESIGN"**
Enclosures	a) REQUISITION LETTER
	b) PERMISSION LETTER
	c) CIRCULAR
	d) SCHEDULE
	e) INVITATION
	f) BROCHURE
	g) LIST OF PARTICIPANTS
	h) FEEDBACK FORM
	i) PHOTO j) CERTIFICATE
No. of Pages	14
Submitted By	**Name : Dr. M.Sangeetha**
	Designation : Professor &HOD/ECE
	Department : ECE
	Signature :

For Office Use Only

Verified By:	K. Sakthivel	Sign:	Date: 24/8/2019
Uploaded By:	K. Senthil Kumar	Sign:	Date: 24/8/2019
File Name:	SEM5 - SEE-ECE - 2019-2020 - 07		

Director, IQAC, BIHER

IQAC Selaiyur

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REQUISITION LETTER

26.07.2019

FROM

The HOD
Department of ECE
Bharath Institute of Higher Education and Research
Selaiyur, Chennai-73

BHARATH INSTITUTE OF HIGHER EDUCATION & RESEARCH
(Declared as Deemed to be University U/S 3 of UGC Act, 1956)
24 AUG 2019
OFFICE OF THE IQAC - BIHER
Selaiyur, Chennai-600 073 INDIA

TO

The Dean Engineering
Bharath Institute of Higher Education and Research
Selaiyur, Chennai-73
Respected Sir,

Subject: Request of Permission to conduct a seminar on **"VERIFICATION TRENDS FOR VLSI DESIGN"** -Reg

With reference to above subject, I would like to bring to your kind notice that, our department interested to organize seminar on **"VERIFICATION TRENDS FOR VLSI DESIGN"** in our campus premises on **22/08/2019** between **10 AM to 1 PM.** In this regard, I kindly request you to grant permission for conducting the same.

Thanking You

HOD/ECE

INSTITUTE OF HIGHER EDUCATION & RESEARCH
Selaiyur, Chennai-600 073. India

Dean Engineering
DEAN (Engineering)
Bharath Institute of Science & Technology
BHARATH INSTITUTE OF HIGHER EDUCATION & RESEARCH
(Declared as Deemed to be University U/S 3 of UGC Act, 1956)
Selaiyur, Chennai-600 073.

Bharath
INSTITUTE OF HIGHER EDUCATION AND RESEARCH
(Declared as Deemed - to - be - University under section 3 of UGC Act 1956)
BHARATH INSTITUTE OF SCIENCE AND TECHNOLOGY
No.173, Agharam Road, Selaiyur, Chennai , T.N - 600 073.

PERMISSION LETTER

29.07.2019

From

The HOD,
Department of ECE,

School of Electrical Engineering,

BIHER.

To
Dr. M.Arun,
Associate Professor
VIT,Vellore

Respected sir,

Sub: - The Department of Electronics and Communication Engineering, School of Electrical Engineering, BIHER, proposed to conduct a SEMINAR in "**VERIFICATION TRENDS FOR VLSI DESIGN**" in our campus premises on **22/08/2019** between **10 AM to 1 PM**"- Permission requested to deliver an invited talk – Reg.

In the continuation of telephonic conversation, it is requested to deliver an invited talk in "**VERIFICATION TRENDS FOR VLSI DESIGN**" in our campus premises on **22/08/2019** between **10 AM to 1 PM**. Kindly accept our request and do the needful .

Convener

Dr.M.Sangeetha
HOD/ECE

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CIRCULAR

SCHOOL OF ELECTRICAL ENGINEERING

Date: 19.08.2019

A Seminar on **"VERIFICATION TRENDS FOR VLSIDESIGN"** is planned by the School of Electrical Engineering on **22/08/2019** between **10 AM to 1 PM.** In this regard, students are instructed to give their willingness and confirm their participation to the program coordinator mention below.

Resource Person:

To
Dr. M.Arun,
Associate Professor
VIT,Vellore

Program Coordinator:

Mrs.S.Saravana

Assistant Professor

Email:selvidurai1975@gmail.com

Contact no:9345475682

Dr.M.Sangeetha
HOD/ECE

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Department of ECE
Program Schedule

Time	Event
09:30 – 10:00 AM	Inaugural Address
10:00 – 10:30 AM	Keynote Address
10:35 – 12.50 PM	Seminar
12:50 – 1:00 PM	Vote of Thanks

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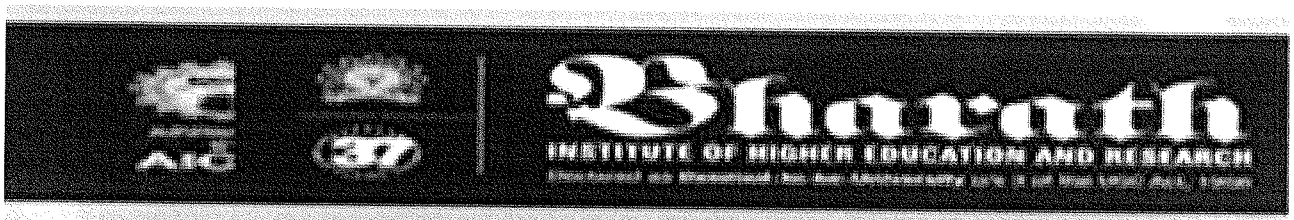
Department of ECE
INVITATION



School of Electrical Engineering
Department of ECE
BHARATH INSTITUTE OF HIGHER EDUCATION AND RESEARCH

SEMINAR ON

VERIFICATION TRENDS FOR VLSI DESIGN

Resource Persons: Dr.Arun,Associate Professor, VIT,VELLORE

Keynote Address: Dr. J. Hameed Hussain, Dean Engineering, BIHER, Chennai
Special Address: Dr. M. Sangeetha, Professor & Head/ ECE, BIHER
Program Coordinator: Ms. G. Jeyalakshmi.

Venue : Smart Room, ECE, BIHER
Date : 22.08.2019
Time : 10.00 am to 1.00 pm

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Department of ECE
Brochure

Registration form:
Name :
Designation:
Name of the Title :

Area of Research :
Organization :
Address for Communication :

Contact No:
Email :
Category : PG students/Research Scholar/Faculty/Industrial person

Payment Details :

D.D No/ Date :
Drawn on Bank :
Amount :

Signature Head of Institution

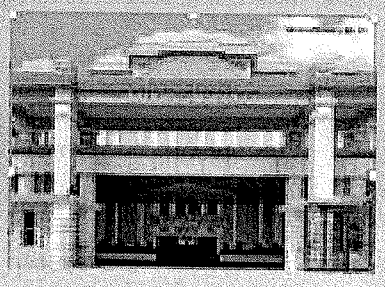
Date :
(Photo copies of the form accepted)

Bharath

BHARATH INSTITUTE OF HIGHER EDUCATION AND RESEARCH
173, Agharam road, Selaiyur, Chennai-600073

National Seminar
on
"Verification Trends for VLSI Design"
22nd August 2019
Organized
by

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING



www.bharathuniv.ac.in

About the University:

The first self-financing Engineering College in the name of Bharath Institute of Science and Technology (BIST) was started in Tamil Nadu in 1984 by Sri Lakshmi Ammal Educational Trust, established by the academic visionary Dr.S.Jagathrakshakan.

Bharath University and is known for providing high-quality education to around 10000 students from across the world in multi-stream. The Institute facilitates the guidance of 1300 teaching faculty members to provide guidance to do Undergraduate, Postgraduate programs and to facilitate Ph.D. research.

About the Department:

Electronics and Communication Engineering (ECE) is a swiftly advancing field, with new ideas emerging every other seconds. Graduate engineers in this discipline will be equipped to design and fabricate, install, operate and maintain complex electronic circuits, equipment's and systems.

The course also covers designing security in communications, besides all the software and hardware required in the communication domain.

About the Seminar:

Verification Trends for VLSI Design is an open source computational software used for assembling components on FPGA, IDD and use defined subroutines for solving complex mathematical problems. This seminar will help participants develop good understanding of computational software and have good hands on experience on how to assemble the different engineering problems using the software. The main focus of the course is on imparting the importance of using such tools and as well making the participants familiar with industry grade problems and solutions in engineering.

Seminar Structure:

Theory of Verification Trends for VLSI Design - Get familiar with

1.What is VLSI DESIGN.
2.Usage of SCADA in Industry
3.Different libraries available in Verification Trends for VLSI Design
4.Developing and compiling a sub-routine with Verification Trends for VLSI Design.

Verification Trends for VLSI Design

We cordially invite the Students, research scholars, Faculties, Industrial persons to explore the various areas of research and to enhance research skill and to enlighten inner aroused work.

Practical Session - Gain hands-on experience by

1. Developing simple sub-routines and compiling them
2. Using in-built libraries to solve common engineering problems
3. Exploring different methods of visualizing
4. Solving industry related engineering problems and devising solutions

Brainstorming session - Solve an assigned problem covering the entire topics on your own at the venue to assess your learning.

The Research scholars and students, Faculties can confirm their registration by sending the DD. The DD should take in favour of "BIHER Chennai" before 13.08.2019, backside of DD carry full name, contact number and address of the author.

Selected candidates list announced through email. Accommodation shall be arranged on request at a reasonable cost.

Dates to be Remember :

Last date for Registration: 17/08/2019

Short Listed candidates list announcement: 20/08/2019.

Registration fee details:

Students : Rs.250/-
Research scholars & Staff members : Rs.500/-
Industry Person : Rs.750/-

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Department of ECE
PARTICIPANTS LIST

S.NO.	REG NO.	NAME OF THE STUDENT
1	U18EC001	AJAY K
2	U18EC002	SEDHURAMAN R
3	U18EC003	VERAMATI SATYANARAYANA
4	U18EC004	NAIDU SIVA KUMAR REDDY
5	U18EC005	KARTHICK M V
6	U18EC006	VARAMATI MOHAN KRISHNA
7	U18EC007	CHUNDRU AVINASH
8	U18EC008	GANGAVARAM DIVYASAI
9	U18EC009	KILARI MURALI
10	U18EC010	POOJARI RAKESH GOUD
11	U18EC011	PATNAM JASWANT
12	U18EC012	DHARSHAN D
13	U18EC014	SURAJ VINAY Y
14	U18EC015	YASHVANTH P
15	U18EC016	S K NIZANTH
16	U18EC017	CHINNAMANAYANAPALLI HARISH KUMAR
17	U18EC018	MOWMITHA S
18	U18EC019	VEDULA GOPINADH
19	U18EC020	LENAKU RUKESWAR REDDY
20	U18EC021	KAVULURI PRAVEEN KUMAR REDDY
21	U18EC022	BANISETTI VINAY KUMAR
22	U18EC023	HANUMANTHU ARAVINDH
23	U18EC024	NEELAM SAICHARAN
24	U18EC025	BOGGULA RAMA KRISHNA REDDY
25	U18EC026	PUTCHAKAYALA PRASAD
26	U18EC027	MONIKA D
27	U18EC028	VOLETI UDEEP
28	U18EC029	MD ZOHAIB
29	U18EC030	VIBIN SRI BALAJI P
30	U18EC031	GADE PAVAN KUMAR REDDY
31	U18EC032	VADDI KRISHNA MOHAN
32	U18EC033	CHINNI BHANU CHANDAR
33	U18EC034	BAKA RAMESH
34	U18EC035	BANDARU RAJESH

35	U18EC036	KOTTE SUNIL KUMAR YADAV
36	U18EC037	VEMULA KESAVA SAI NAGESH
37	U18EC038	ANNEM VINAY KUMAR REDDY
38	U18EC039	GANGULA SATEESH CHANDRA
39	U18EC040	CHITTURI YUVA KIRAN
40	U18EC041	GUTHA MAHESH

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Department of ECE

PHOTOS

" Verification Trends for VLSI Design" dated on 22.08.2019 between 10.00 AM to 1.00 PM

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Department of ECE
CERTIFICATE

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NAAC

ABET

SCHOOL OF ELECTRICAL ENGINEERING

CERTIFICATE OF PARTICIPATION

This is to certify that Mr/ Ms. SURAJ VINAY.J (U18EC014) has attended SEMINAR On **"Verification Trends For VLSI Design"** organized by the School of Electrical Engineering, BIHER conducted on **22-08-2019.**

Ms.G.JEYALAKSHMI
COURSECOORDINATOR

Dr.M.SANGEETHA
CONVENOR

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SCHOOL OF ELECTRICAL ENGINEERING
FEEDBACK FORM
SEMINAR ON VERIFICATION TRENDS FOR VLSI DESIGN

FEED BACK FORM

Date: 22.08.2019

Name	S. K. Nizanth
Phone number	9686391900

	Poor	Fair	Good	Very Good	Excellent
Overall Program				✓	
The Speaker				✓	
Audio, Visual Aids Technology used				✓	
Presentation hand outs					✓

Student Signature

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SCHOOL OF ELECTRICAL ENGINEERING

FEEDBACK FORM

SEMINAR ON VERIFICATION TRENDS FOR VLSI DESIGN

FEED BACK FORM					Date: 22.08.2019
Name	Dharshan D				
Phone number	9003001411				
	Poor	Fair	Good	Very Good	Excellent
Overall Program			✓		
The Speaker			✓		
Audio, Visual Aids Technology used				✓	
Presentation hand outs					✓

D. Dharshan.

Student Signature