Bharath
INSTITUTE OF HIGHER EDUCATION AND RESEARCH

(Declared as Deemed-to-be University under section 3 of UGC Act, 1956)
(Vide Notification No. F.9-5/2000 - U.3, Ministry of Human Resource Development, Govt. of India, dated 4th July 2002)

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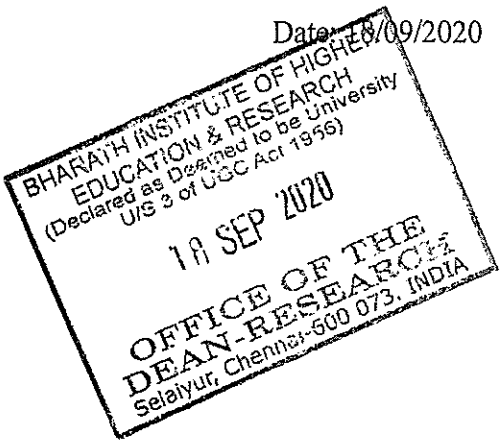
Chennai - 600 073. Tamil Nadu.

Ref No.SMS-2018-O-13

Date: 18/09/2020



TO

Mrs. Jasmin,

Associate Professor/ECE,

BIHER.

Thro: Concern Head of the Department

Greetings!!!

We are happy to announce that the Research Advisory Committee has approved your proposal for Seed Money Scheme-2018 which was presented by you. You are requested to complete the proposal and send the progress report to the Dean Research in the prescribed time period.

Title of the Project: Adaptive Low power Coding Schemes for Efficient Realization of Network On Chip

Seed Money Amount: Rs.1, 00,000/- (Rupees One Lakh Only)

Approved on: 10/03/2020

Payment details:

Cheque No.351642 **Dated: 16/09/2020**

Bank Name: Indian Bank, Selaiyur, Chennai.

With Regards

Dean-Research

इंडियन बैंक
Indian Bank

Branch : SELAIYUR (TAMBARAM)
PLOT NO.17 AND 18, HASAN COLONY
AGARAM ROAD, SELAIYUR.,TAMBARAM. CHENNAI. T.N.
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VALID FOR THREE MONTHS ONLY

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PAY Ms. M. Jasmin या धारक को OR BEARER

RUPEES रुपये One Lakh Only

अदा करें ₹ 1,00,000/-

खा.सं. A/c No.	CA 6670628110

FOR BIHER RESEARCH AND CONSULTANCY

CBS Code: 02505

AUTHORISED SIGNATORY

992000069

PAYABLE AT PAR AT ALL OUR BRANCHES

Please sign above

⑈351642⑈ 600019250⑆ 628110⑈ 29

PROPOSAL SUBMISSION

1. **Details of Principal Investigator**

Name	: M.Jasmin
Designation	:Associate Professor
Highest Qualifications	:M.Tech(Ph.D)
Department	:Electronics and Communication Engineering
E-mail	:jasmine.ece@bharathuniv.ac.in
Contact no	:9445240930
Date of Joining	:7.7.2009

2. **Details of Co - Principal Investigator**

Name	:Dr.B.Karthik
Designation	:Associate Professor
Highest Qualifications	:Ph.D.
Department	:Electronics and Communication Engineering
E-mail	:karthik.ece@bharathuniv.ac.in
Contact no	:9842580740
Date of Joining	:17.9.2007

TECHNICAL DETAILS

1. Introduction

Low power system design is important one for the system on chip design where many sub system blocks communicate with each other with higher data rate in order to realize the system functionality. Low power coding either will reduce energy by reducing self-switching activity or reduces energy consumption by reducing coupling switching activity. But under typical NOC system we require a low power coding scheme which has to handle different kind of data traffic that comes from different IP core at different instant at different places in the SOC. A single low power coding will not solve all the subsystem or application demands. So here in this research a correlation analysis based adaptive data coding scheme is presented which will provide low power at any instant on any kind of data traffic by selecting and encoding the data with different coding scheme based on correlation level of the data traffic.. The proposed system has to be simulated in labview FPGA tool for the USRP RIO target which is a wireless transceiver that can inject megabits of test data per second for testing the coding scheme .The power consumption of the coding schemes are compared with the proposed adaptive scheme by taking different correlation based test data sets.

Under system on chip design the number of integrated cores to realize the system is rapidly increasing ever. Because of the increased core in the system the interconnection system and the inter core communication becomes more important. The on-chip communication techniques on the interconnect will be the limiting factors for performance and power consumption in SoCs.The efficient interconnect technology for this highly complex SOC with many cores can be realized by means of NoCArchitectures. Performance, consumption of power and reliability are the three key design parameter which should be optimized in the NOC based SOC.Among the three parameters the power consumption is considered more because of the increased core in the system

design. Power consumption is more in the interconnect technology of NOC rather than the processing core elements.

There are many approaches to reduce the power consumption in the link. The data encoding scheme is the straight forward method that will be reducing the dynamic switching power in the data transmission in the link. Under typical SOC the different IP core will generate different type of data traffic at different instant of time .So a single coding scheme will not guarantee to reduce the energy consumption in the SOC system. So there is a need for an adaptive data encoding scheme that will encode the data based on the nature of the data traffic .Here in this research such an adaptive encoding scheme which will encode the data on the basis of correlation index of data traffic is proposed. This will reduce the energy consumption.

2. Review of status of Research and Development in the subject

- **Data Encoding Techniques For Reducing Energy Consumption In Network-On-Chip**

NimaJafarzadeh Department of Computer Science, ,Tehran, Iran, Maurizio Palesi,Kore University of Enna, Italy , Ahmad Khademzadeh, Iran Telecommunication Research Center, Tehran, Iran. .AliAfzali-Kusha, College of Engineering, School of Electrical and Computer Engineering, Tehran, Iran

As technology shrinks, the power dissipated by the links of a network-on-chip (NoC) starts to compete with the power dissipated by the other elements of the communication subsystem, namely, the routers and the network interfaces (NIs). In this paper, we present a set of data encoding schemes aimed at reducing the power dissipated by the links of an NoC. The proposed schemes are general and transparent with respect to the underlying NoC fabric (i.e., their application does not require any modification of the routers and link architecture). Experiments carried out on both synthetic and real traffic scenarios show the effectiveness of the proposed schemes, which allow to save up to 51% of power dissipation and 14% of energy consumption without any significant performance degradation and with less than 15% area overhead in the NI.

- **Silent: Serialized Low Energy Transmission Coding For On-Chip Interconnection Networks**

Kangmin Lee, Korea Advance Institute of Science and Technology,Daejeon,South Korea Seejong Lee, Korea Advance Institute of Science and Technology, Daejeon, South Korea , HoijunYoo, Korea Advance Institute of Science and Technology, Daejeon, South Korea.

On-chip source-synchronous serial communication has many advantages over multi-bit parallel communication in the aspects of skew, crosstalk area cost, wiring difficulty, and clock synchronization. However, the serial wire tends to dissipate more energy than parallel bus due to the bit multiplexing. We propose a coding method to reduce the transmission energy of the serial communication by minimizing the number of transitions on the serial wire. We demonstrate the significant energy saving in a multimedia application, 3D graphics. We also apply the coding technique to a CMOS SoC implementation which integrates various processing units with packet switched on-chip networks.

- **A Variable Frequency Link For A Power Aware Network-On-Chip (NOC)**

S. E. Lee and N. Bagherzadeh

An energy-efficient network-on-chip (NoC) is presented for possible application to high-performance system-onchip (SoC) design. It incorporates heterogeneous intellectual properties (IPs) such as multiple RISCs and SRAMs, a reconfigurable logic array, an off-chip gateway, and a 1.6-GHz phase-locked loop (PLL). Its hierarchically-star-connected on-chip network provides the integrated IPs, which operate at different clock frequencies, with packet-switched serial-communication infrastructure. Various low-power techniques such as low-swing signaling, partially activated crossbar, serial link coding, and clock frequency scaling are devised, and applied to achieve the power-efficient on-chip communications. The 5 5 mm2 chip containing all the above features

is fabricated by 0.18- m CMOS process and successfully measured and demonstrated on a system evaluation board where multimedia applications run.

- **Low-Power And High-Performance Adaptive Routing In On-Chip Networks**

  Dong Xiang Tsinghua University, Beijing & Qunyang Pan Tsinghua University, Beijing

Performance and power are two conflict requirements in a NoC. It is attractive to propose a low-power and high-performance routing scheme. A new low-power fully adaptive routing algorithm is proposed for virtual cut-through or wormhole switched networks-on-chip. The following new techniques are proposed: (1) multiple packets can be delivered across the same physical channel via different bypassing channels, (2) a low-power bypassing hop can include both x and y channels, (3) a new low-power routing selection function is defined for more power reduction, (4) a new limited-global control signaling scheme is proposed, (5) a new cycle-accurate system-level power estimation model is proposed, and (6) bypassing hops of any lengths and the normal hops in the original network can share the same virtual channels. Simulation results are presented to evaluate the performance and power by comparison with some previous methods.

- **Encoding Technique For Reducing Power Dissipation In Network On Chip Serial Links**

  Deepa N.Sharma , G.Lakshminarayanan, National Institute of Technology,Trichy

The interconnects have become main element in dynamic power dissipation in a Network on Chip (NoC) design. Though there have been much work on reduction of switching activity in a link, few techniques have been discussed in serial coding. In SILENT coding, the effectiveness of data dependent technique is studied. In this paper, a data independent technique is proposed in which number of switching transitions in a data word is brought down to a threshold level by rearranging data bits. To verify the efficacy of the proposed technique, encoder and decoder structures

are designed using the proposed technique and described in RTL level in Verilog HDL, synthesized and mapped into UMC180 nm technology library. Proposed technique offers a maximum reduction in dynamic power consumption of 45.92%. In cases where the correlation between successive data bits is low, SILENT coding introduces an overhead in peak power consumption. It is proved that application of proposed technique with SILENT coding eliminates this overhead. The static power dissipation in proposed structure is negligible and can be easily compensated by reduction in power consumption in NOC links. In comparison with simple structure of SILENT encoder there is an overhead area of about 41.2% in structure of encoder. Proposed encoder was analyzed with various types of data streams and results confirm that unlike SILENT coding, significant power reduction is guaranteed in all the cases.

- **Reducing Energy Consumption InNoc By Data Encoding And Decoding Techniques**

ChaithraK,Veena S Murthy B N M Institute Of Technology, Bangalore

This work mainly focuses on reducing the consumption of energy by the power dissipated links of a networkon-chip (NoC - Network on Chip) which starts to compete with the power dissipated by the other elements of the communication subsystem like the routers and the network interfaces (NIs). It provides a set of data encoding and decoding schemes aimed at reducing the power dissipated by the links of a NoC. The proposed schemes are general and transparent with respect to the underlying NoC Architectures. The paper provides few techniques to overcome the power dissipation by self switching activity and coupling switching activity. The proposed schemes has been implemented on Xilinx FPGA of Spartan-6 Family and it shows that 51% of power dissipation and 14% of energy consumption is saved and 15% area overhead in the NI is achieved without affecting the performance.

2.1 National Status

Nil

2.2 International Status

Nil

3. **Progress/achievement so far,**

a) Literature review was done

b) Methodology was designed for the identified problem

c) Proposed work has been started in developing adaptive coding schemes for efficient realization of Network on Chip

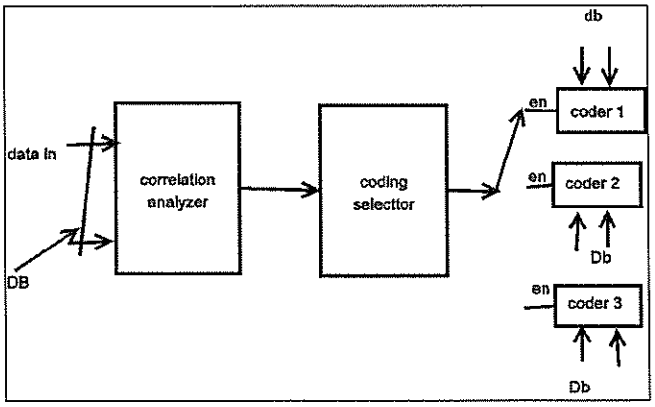
4. **Work Plan:**

4.1 Methodology:

The main objectives of the adaptive coder for Network On Chip are as follows,

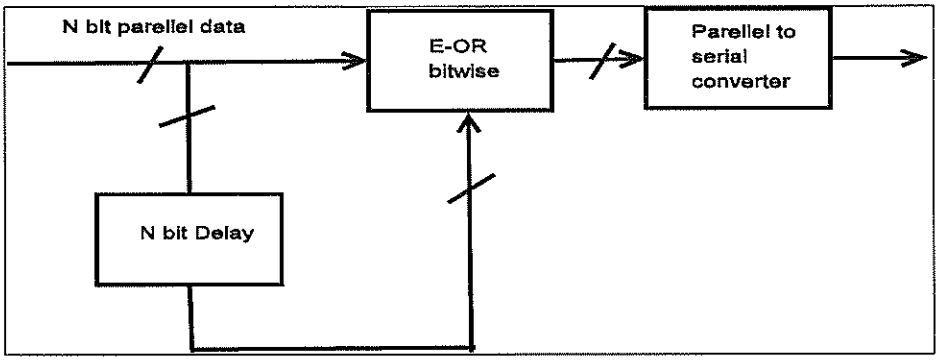
- To develop the proper coding schemes for each data type
- To analysis the performances of designed coding schemes
- To design and simulate the coder for low correlated data to estimate the area and power consumption.
- To design and simulate the coder for medium correlated data to estimate the area and power consumption
- To design and simulate the coder for high correlated data to estimate the area and power consumption
- To analyse the various resource utilization and energy consumption of the adaptive coder designed for Network On Chip.

Block Diagram:



Block Diagram of Low Power Adaptive Coder

Coding Scheme	SILENT	Bit Inverting Code	Self Switching Activity Reduction Code
Correlation	High Correlation	Moderate Correlation	Low Correlation

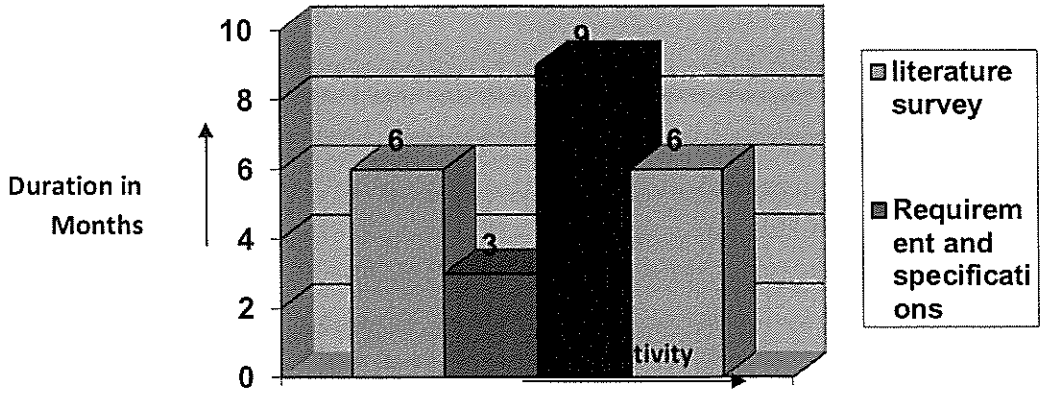


Functional block diagram of SILENT code

4.2 Time Schedule of activities giving milestones through BAR diagram.

Work plan (including detailed methodology and time schedule)

Sl. No.	Activity / Milestone	1st Year		2nd Year	
1.	Literature Survey	**1-6**			
2.	Requirements and Specification analysis		**7-9**		
3.	Designing the methodology			**10-18**	
4.	Testing the output				**19-24**



4.3 Expected outcome within the time period of Seed Money Scheme

a) The adaptive coder will be designed and simulated within the time period of Seed Money Scheme.

b) The Proposed system will be tested for Communication data traffic of USRP RIO transmitter data sets. within the time period of Seed Money Scheme.

5 Suggested Plan of action stating the name of funding agency where the project will be communicated for financial support within the time period of project.

Nil

6 Bibliography:

1. Benini, L. et al. (1997) 'Asymptotic zero-transition activity encoding for address busses inlowpower microprocessor-based systems', in Proc. of Great Lakes Symp. on VLSI, pp.77–82,March.
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technologies', IPSJTrans. Syst. LSI Design Methodol., August, Vol. 1, pp.2–17

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7 List of Projects submitted/implemented by the Investigators (Separate for Pi and Co-PI)

Nil

7.1 Details of Projects submitted to various funding agencies:

SI.NO	Title	Cost in Lakhs	Month of Submission	Role of PI/Co-PI	Agency	Status
	NA	NA	NA	NA	NA	NA

7.2 Details of Projects under implementation

SI.NO	Title	Cost in Lakhs	Duration	Role of PI/Co-PI	Agency
	NA	NA	NA	NA	NA

7.3 Details of Projects Completed during the last 5 Years

SI.NO	Title	Cost in Lakhs	Duration	Role of PI/Co-PI	Agency
	NA	NA	NA	NA	NA

8 List of publications published by the Investigators, if any:

a) Co - Principal Investigator

S.No	Author names	Title of paper	Name ofJournal	Vol (issue)	Page no.	Year
1.	Arulselvi, S. Karthik, B. Sundararajan, M,	Modeling and Simulation Capacity Analysis of MIMO Wireless Sensor Network	Journal Of Mechanics Of Continua And Mathematical Sciences	Special Issue, No.-2	236-245	2019
2.	Karthik, B. Jasmin, M. Arulselvi S.	Real Concern to High Speed VLSI Design for Interconnect Scaling	Journal Of Mechanics Of Continua And Mathematical Sciences	Special Issue, No.-2	457-463	2019
3.	Karthik, B. Philomina, S Jasmine	BIST for reconfigurable system on chip (SOC) for micro-vibration measurement	International Journal of Engineering and Advanced Technology	8(6)	67-70	2019
4.	Karthik, B. Sriram, M. Sidharth Raj, R.S.	Authentication of bi-level QR code with dynamic pattern generation	International Journal of Engineering and Advanced Technology,	8(6)	346-350	2019
5.	Karthik, B., MeenaKumari, G., Jasmin, M., Arulselvi, S.,	Intermittently associated mobile cognitive radio networks using portability assisted routing	International Journal of Engineering and Advanced Technology	8(Special Issue 2)	71-74	2019
6.	GowriSankaran, B., Karthik, B., Vijayaragavan, S.P.,	Entropy based estimation algorithm using break-up images to decrease loss compression ratio.	International Journal of Recent Technology and Engineering	8(2)	4700-4703	2019
7.	Vaidianathan, B., Arul Selvi,	A stochastic analysis on translating Nam speech into	International Journal of			

	S., Karthik, B	normal speech, International Journal of Recent Technology and Engineering	Applied Engineering Research	7(5)	839-842	2019
8.	Manik, K.R., Arulselvi, S.,Karthik, B.	Granular traffic analysis and energy modeling in NoC with enhanced data transmission	International Journal of Innovative Technology and Exploring Engineering	8(5)	352-362	2019
9.	Manik, K.R., Arulselvi, S.,Karthik, B.	Designing network interface component for peripheral IP cores in networks-on-chip	International Journal of Innovative Technology and Exploring Engineering	8(4)	329-336	2019
10.	Karthik, B., Sundararajan, M	Integer wavelet transform utilized SVC-H.264 standard for medical video compression,	Journal of Chemical and Pharmaceutical Sciences	9(3)	S266-S269	2016
11.	Karthik, B., Susila, M., Sundararajan, M.,	Talking navigation cane with moveable braille note taker for visually impaired, , V-9, I-3, pp-S279-S282, 2016.	Journal of Chemical and Pharmaceutical Sciences	9(3)	S279-S282	2016
12.	Thamarai, P., Karthik, B.,	Effect of feature fusion for PF tumor segmentation with modified ams algorithm	Middle - East Journal of Scientific Research	20(12)	2245-2251	2014
13.	Philomina, S., Karthik, B.,	Wi-Fi energy meter implementation using embedded linux in ARM	Middle - East Journal of Scientific Research	20(12)	2434-2438	2014
14.	Karthik, B., Arulselvi,	Test data compression architecture for lowpowervlsi	Middle - East Journal of	20(12)	2331-2334	2014

	Selvaraj, A.,	testing	Scientific Research			
15.	Karthik, B., Kumar, T.V.U.K.,	Authentication verification and remote digital signing based on embedded arm (LPC2378) platform	World Applied Sciences Journal	29(9)	1170-1174	2014
16.	Dolphin Kiruba, D., Karthik, B.,	Development of period extension and randomness using RM-PRNG, , V-9, I-22, pp-6194-6201, 2014.	International Journal of Applied Engineering Research	9(22)	6194-6201	2014
17.	Nirosha, R., Karthik.B	Increasing the system efficiency using contactless power transfer system	International Journal of Applied Engineering Research	9(22)	6456-6462	2014
18.	Kiran Kumar, T.V.U., Karthik, B., Bharath Kumaran, E.,	Implementation of a can-based digital driving system for a vehicle, V-13, I-12, pp-1564-1569, 2013	Middle - East Journal of Scientific Research	13(12)	1564-1569	2013
19.	Karthik, B., Kiran Kumar, T.V.U., Vijayaragavan, P., Bharath Kumaran, E,	Design of a digital PLL using 0.35µm CMOS technology	Middle - East Journal of Scientific Research	18(12)	1803-1806	2013
20.	Karthik, B., Kiran Kumar, T.V.U., Bharath Kumaran, E,	Visual secret sharing scheme for JPEG compressed images	Middle - East Journal of Scientific Research	12(12)	1873-1880	2012

b) Principal Investigator

S.No	Author names	Title of paper	Name ofJournal	Vol (issue)	Page no.	Year
1	M.Jasmin T.Vigneswaran	An adaptive low power coding scheme for the NoC	International Journal of Advanced Intelligence Paradigms	13(3-4)	324-333	2019
2	Karthik B Meena Kumari M Jasmin M	Archimedean antenna design with ultra-ease "Green" module	International Journal of Engineering and Advanced Technology	8(6 Special Issue 2)	358-361	2019
3	Jasmin M Angelo Virgin G.Jeyalakshmi	Design and implementation of WIFI controlled robotic rover based on raspberry-pi and Arduino	International Journal of Recent Technology and Engineering	8(1)	22-25	2019
4	.Jasmin M Ramya S Hemalatha B	Design of multi robots based on single master commands	International Journal of Engineering and Advanced Technology	8(6 Special Issue 2)	191-194	2019
5	Karthik B. Hemalatha Jasmin M	Enhancement of satellite imagesusing image sharpening technique	International Journal of Engineering and Advanced Technology	8(6 Special Issue 2)	351-354	2019
6	Karthik B, Meena Kumari G, Jasmin M	Intermittently associated mobile cognitive radio networks using portability assisted routing	International Journal of Engineering and Advanced Technology	8(6 Special Issue 2)	71-74.	2019
7	Jasmin M Manoj S Meenaa Kumari	Leaf disease analysis using smart system	International Journal of Engineering and Advanced Technology	8(6 Special Issue 2)	362-367	2019
8	Karthik B Sriram M Jasmin M	Low power and high performance MTCMOS conditional discharge flip flop,	International Journal of Engineering	8(6 Special Issue 2)	341-345	2019

			and Advanced Technology			
9	Jasmin M Philomina S Arulselvi S	Neighbor discovery in ASN.	International Journal of Innovative Technology and Exploring Engineering	8(9 Special Issue 3)	628-630	2019
10	Philomina S Jasmin M Sathya Narayan R	Passive IP trace back using Border Gateway Protocol (BGP)	International Journal of Innovative Technology and Exploring Engineering	8(9 Special Issue 3)	1140-1144	2019
11	Jasmin M Saravana S Kanagavalli G	RFID security and privacy enhancement .	International Journal of Engineering and Advanced Technology	8(6 Special Issue 2)	319-322	2019
12	Karthik B Jasmin M Arulselvi S	Stacking technique for low power SRAM	International Journal of Engineering and Advanced Technology	8(6 Special Issue 2)	118-121	2019
13	Karthik B Hemalatha S Jasmin M	Wireless voice controlled cursor control using RF	International Journal of Engineering and Advanced Technology	8(6 Special Issue 2)	355-357	2019
14	M. Jasmin, S. Philomina	Runtime adaptive Dynamic Voltage Frequency Scaling technique for reducing the power consumption in Multi Processor System On Chip	Journal of Mechanics of Continua and Mathematical Sciences	Special Issue, No.-2	275-285	2019.
15	M. Jasmin Vigneswaran T.	Fuzzy based adaptive controller for on - Chip communication	International Journal of Engineering and Technology	7(3.27)	362-367	2018.
16	S.BeulahHemalatha M.Jasmin	A new approach to reduce leakage current in 6t SRAM using finfet	Journal of Chemical and Pharmaceutical sciences	9(3)	234-238	2016

17	S.BeulahHemalatha, T.Vigneshwaran, M.Jasmin	Survey on Energy efficient Methodologies and architectures of Network-on-Chip	Indian Journal of Science and Technology	9(12)	1-8	2016
18	.M.Jasmin	Design Of Power Aware On Chip Embedded Memory Based FSM Encoding In FPGA.	International Journal of Applied Engineering Research	10(2)	4487-4496	2015
19	M.Jasmin	Perception Drug case that admonishes correct Dosing	Middle-East Journal of Scientific Research	20 (11)	1924-1928	2014
20	.M.Jasmin	Optimization Techniques for Low Power VLSI Circuits",	Middle-East Journal of Scientific Research	20(9)	1082-1087	2014.

9. **Budget**

Sl. No.	Equipment	Quantity	Amount in INR
1	NI USRP-2940R, 120MHz BW, 50 MHz TO 2.2 GHz SDR	1	43,000
	Artix 7 FPGA Kit	1	22,000
2	Consumables (Like, testing tools Charge controller, etc.)	As per requirement	20,000
3	Travel support for the purpose of research work.	---	5,000
4	Contingency	---	5000
5	Others	---	5000
	Total		1,00,000

10. **Name of at least two subject experts from the Institute and one from the outside Institute with their contact details:**

a) Dr.M.Sangeetha – Professor& Head, Dept of ECE, BIHER, Chennai-600073.

b) Dr.M.Manikandan – Associate Professor, Dept of ECE, MIT Campus,Chennai

CERTIFICATE FROM THE INVESTIGATOR

Project Title: Adaptive Low power Coding Schemes for Efficient Realization of Network On Chip

It is certified that

1. I do hereby agree to submit a complete proposal for financial support to the external funding agency within the time period of SMS-2018

2. I undertake that spare time on equipment procured in the project will be made available to other users.

3. I agree to submit a certificate from Institutional Biosafety Committee, if the project involves the utilization of genetically engineered organisms. I also declare that while conducting experiments, the Biosafety Guidelines of Department of Biotechnology, Department of Health Research, GOI would be followed in to.

4. I agree to submit ethical clearance certificate fom the concerned ethical committee,if the project involves field trials/experiments/exchange of specimens.human& animal materials etc.

5. I agree to abide by the terms and conditions of SMS-2018, BIHER, and Chennai.

M. Jasmin

Name and signature of
Principal Investigator

(M. JASMIN)

B. Karthik

Name and signature of
Co-Principal Investigator

(DR. B. KARTHIK)

Date: 06.1.2020
Place: Chennai - 73

Forwarded by Head of the Department

Signature of the Head

PROJECT EVALUATION FORMAT

Recommendation Sheet

Name of the Principal Investigator	Ms M.Jasmin
Name of the Co-Investigator	Dr.B.Karthik
Name of the Department	ECE
Title of project	Adaptive Low power Coding Schemes for Efficient Realization of Network On Chip
Recommendation of the evaluation committee	Recommended
Financial allocation recommended	Rs. 1,00,000/-

Sl. No.	Equipment	Quantity	Amount in INR
1	NI USRP-2940R, 120MHz BW, 50 MHz TO 2.2 GHz SDR	1	43000
	Artix 7 FPGA Kit	1	22,000
2	Consumables	As per requirement	20,000
3	Travel support for the purpose of research work.	---	5,000
4	Contingency	---	5000
5	Others	---	5000
	Total		1,00,000

Name and Signature of the Research Advisory Committee members with date

Dr. P. Naveenchandran

Internal Quality Assurance Cell IQAC Selaiyur Chennai-73 BIHER