Academic Course Description

BHARATH UNIVERSITY
Faculty of Engineering and Technology
Department of Electrical and Electronics Engineering
BEE604 Digital Signal Processing
Six Semester (Even Semester)

Course (catalog) description

- To classify signals and systems& their mathematical representation.
- To analyze the discrete time systems.
- To study various transformation techniques & their computation.
- To study about filters and their design for digital implementation.
- To study about a programmable digital signal processor & quantization effects

Compulsory course **:** Compulsory for EEE students

Credit hours& contact hours: 3& 45 hours

Course Coordinator : Dr.S.P.Vijayaragavan

Instructors **:** Dr.S.P.Vijayaragavan

Name of the instructor	Class handling	Office location	Office phone	Email (domain:@ bharathuniv.ac.in	Consultation
Dr.S.P.Vijayaragavan	Third year EEE	KS 302	**04422290125**	sherine07@gmail.com	12.30-1.30 PM

Relationship to other courses:

Pre –requisites **:**BMA301 - Mathematics – III

Assumed knowledge : The student has basic knowledge in solving Z-transform, discrete fourier transform in his Mathematical papers.

Syllabus Contents

UNIT I INTRODUCTION 9

Classification of systems: Continuous, discrete, linear, causal, stable, dynamic, recursive, time variance; classification of signals: continuous and discrete, energy and power; mathematical representation of signals; spectral density; sampling techniques, quantization, quantization error, Nyquist rate, aliasing effect. Digital signal representation.

UNIT II DISCRETE TIME SYSTEM ANALYSIS 9

Z-transform and its properties, inverse z-transforms; difference equation – Solution byztransform, application to discrete systems - Stability analysis, frequency response – Convolution – Fourier transform of discrete sequence – Discrete Fourier series.

UNIT III DISCRETE FOURIER TRANSFORM & COMPUTATION 9

DFT properties, magnitude and phase representation - Computation of DFT using FFT algorithm – DIT & DIF - FFT using radix 2 – Butterfly structure.

UNIT IV DESIGN OF DIGITAL FILTERS 9

FIR & IIR filter realization – Parallel & cascade forms. FIR design: Windowing Techniques – Need and choice of windows – Linear phase characteristics. IIR design: Analog filter design - Butterworth and Chebyshev approximations; digital design using impulse invariant and bilinear transformation - Warping, prewarping – Frequency transformation.

UNIT V DIGITAL SIGNAL PROCESSORS 9

Introduction – Architecture – Features – Addressing Formats – Functional modes - Introduction to Commercial Processors

Text book(s) and/or required materials

T_1.J.G. Proakis and D.G. Manolakis, 'Digital Signal Processing Principles, Algorithms and Applications', Pearson Education/ PHI, 4th Edition, New Delhi, 2007.

T_2.S.K. Mitra, 'Digital Signal Processing – A Computer Based Approach', Tata McGrawHill, 3rd Edition, New Delhi, 2008.

Reference Books:

R1.Alan V. Oppenheim, Ronald W. Schafer and John R. Buck, 'Discrete – Time Signal Processing', Pearson Education, New Delhi, 2003.

R2.Emmanuel C Ifeachor and Barrie W Jervis ,"Digital Signal Processing – A Practical Alan V. Oppenheim, Ronald W. Schafer and John R. Buck, 'Discrete – Time Signal Processing', Pearson Education, New Delhi, 2003.

Approach" Pearson Education, Second edition, 2002.

R3.Steven W. Smith, "The Scientist and Engineer's Guide to Digital Signal Processing", Second Edition, California Technical Publishing San Diego, California.www.DSPguide.com)

R4.B. Venkataramani, M. Bhaskar, 'Digital Signal Processors, Architecture, Programming and Applications', Tata McGraw Hill, New Delhi, 2003

Computer usage:

Professional component

General	-	0%
Basic Sciences	-	0%
Engineering sciences & Technical arts	-	0%
Professional subject	-	100%

Test Schedule

S. No.	Test	Tentative Date	Portions	Duration
1	Cycle Test-1	February 2nd week	Session 1 to 18	2 Periods
2	Cycle Test-2	March 2nd week	Session 19 to 36	2 Periods
3	Model Test	April3rd week	Session 1 to 45	3 Hrs
4	University Examination	TBA	All sessions / Units	3 Hrs.

Mapping of Instructional Objectives with Program Outcome

	Correlates to program outcome		
	H	**M**	**L**
1. Explain Properties and algorithms for implementation of DFT.	a,b,d,h,I,j,k,l	c,g	e,f,h
2. Filters Describe and their structures.	a,d,c,d,e	m	f
3. Illustrate the design of FIR and IIR filters.	a,b,c,d,e,h,I,j,k,l		
4. Describe the quantization effects.	d,h,i,k	a,b,e,l	c
5. Relate the architectures and instruction set of a Digital Signal Processor.	a,b,c,d,e,h,i,l	f,g	

H: high correlation, M: medium correlation, L: low correlation

Draft Lecture Schedule

S.NO	Topics	Problem solving (Yes/No)	Text / Chapter
UNIT I	**INTRODUCTION**		
1.	Classification of systems - discrete, linear, Causal	**Yes**	$[T_1]$ & $[T_2]$
2.	Classification of systems - stable, dynamic, recursivetime variance	**Yes**	
3.	classification of signals - continuous and discrete	**Yes**	
4.	classification of signals - energy and power	**Yes**	
5.	mathematical representation of signals, spectral density	**Yes**	
6.	sampling techniques	**Yes**	
7.	quantization error	**Yes**	
8.	Nyquist rate, aliasing effect	**Yes**	
9.	Digital signal representation	**Yes**	
UNIT II	**DISCRETE TIME SYSTEM ANALYSIS**		
10.	Z-transform and its properties	**Yes**	$[T_1]$ & $[T_2]$
11.	inverse z-transforms	**Yes**	
12.	difference equation Solution byztransform	**Yes**	
13.	Stability analysis	**Yes**	
14.	frequency response	**Yes**	
15.	Convolution	**Yes**	
16.	Fourier transform of discrete sequence	**Yes**	
17.	Discrete Fourier series	**Yes**	
18.	Extra Problems	**Yes**	
UNIT III	**DISCRETE FOURIER TRANSFORM & COMPUTATION**		
19.	DFT properties	**Yes**	$[T_1]$ & $[T_2]$
20.	Magnitude and Phase representation	**Yes**	
21.	Computation of DFT using FFT algorithm	**Yes**	
22.	DIT - FFT using radix 2	**Yes**	
23.	DIF - FFT using radix 2	**Yes**	
24.	Butterfly structure - problems	**Yes**	
25.	Extra problems	**Yes**	
26.	Extra problems	**Yes**	
27.	Review of unit III	**Yes**	
UNIT IV	**DESIGN OF DIGITAL FILTERS**		
28.	FIR filter realization	**Yes**	$[T_1]$ & $[T_2]$
29.	IIR filter realization	**Yes**	
30.	FIR design Windowing Techniques	**Yes**	
31.	Parallel & cascade forms	**Yes**	
32.	Need and choice of windows Linear phase characteristics.	**Yes**	
33.	Analog filter	**Yes**	

	designButterworthapproximations		
34.	Analog filter designChebyshev approximations	**Yes**	
35.	Digital design using impulse invariant and bilinear transformation	**Yes**	
36.	Warping, prewarping – Frequency transformation.	**Yes**	
UNIT V	**DIGITAL SIGNAL PROCESSORS**		
37.	Introduction to processors	No	
38.	Architecture&Features	No	
39.	Addressing Formats	No	
40.	Functional modes	No	
41.	Introduction to Commercial Processors	No	$[T_1]$ & $[T_2]$
42.	Review of UNIT -I V	Yes	
43.	Review of UNIT - V	No	
44.	Surprise test		
45.	Discussion for University Exam		

Teaching Strategies

The teaching in this course aims at establishing a good fundamental understanding of the areas covered using:

- Formal face-to-face lectures
- Tutorials, which allow for exercises in problem solving and allow time for students to resolve problems in understanding of lecture material.
- Laboratory sessions, which support the formal lecture material and also provide the student with practical construction, measurement and debugging skills.
- Small periodic quizzes, to enable you to assess your understanding of the concepts.

Evaluation Strategies

Cycle Test – I	-	05%
Cycle Test – II	-	05%
Model Test	-	10%
Attendance	-	05%
SEMINAR&ASSIGNMENT	-	05%
Final exam	-	70%

Prepared by: Dr.S.P.Vijayaragavan **Dated :**

Addendum

ABET Outcomes expected of graduates of B.Tech / EEE / program by the time that they graduate:

a) An ability to apply knowledge of mathematics, science, and engineering fundamentals.
b) An ability to identify, formulate, and solve engineering problems.
c) An ability to design a system, component, or process to meet the desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.
d) An ability to design and conduct experiments, as well as to analyze and interpret data.
e) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.
f) An ability to apply reasoning informed by the knowledge of contemporary issues.
g) An ability to broaden the education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context.
h) An ability to understand professional and ethical responsibility and apply them in engineering practices.
i) An ability to function on multidisciplinary teams.
j) An ability to communicate effectively with the engineering community and with society at large.
k) An ability in understanding of the engineering and management principles and apply them in project and finance management as a leader and a member in a team.
l) An ability to recognize the need for,and an ability to engage in life-long learning.

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Program Educational Objectives

PEO1: PREPARATION
Electrical Engineering Graduates are in position with the knowledge of Basic Sciences in general and Electrical Engineering in particular so as to impart the necessary skill to analyze and synthesize electrical circuits, algorithms and complex apparatus.

PEO2: CORE COMPETENCE
Electrical Engineering Graduates have competence to provide technical knowledge, skill and also to identify, comprehend and solve problems in industry, research and academics related to power, information and electronics hardware.

PEO3: PROFESSIONALISM
Electrical Engineering Graduates are successfully work in various Industrial and Government organizations, both at the National and International level, with professional competence and ethical administrative acumen so as to be able to handle critical situations and meet deadlines.

PEO4: SKILL
Electrical Engineering Graduates have better opportunity to become a future researchers/ scientists with good communication skills so that they may be both good team-members and leaders with innovative ideas for a sustainable development.

PEO5: ETHICS
Electrical Engineering Graduates are framed to improve their technical and intellectual capabilities through life-long learning process with ethical feeling so as to become good teachers, either in a class or to juniors in industry.

Course Teacher	Signature
Dr.S.P.Vijayaragavan	

Course Coordinator **HOD/EEE**

(Dr.S.P.Vijayaragavan) ( )