UNIT I

The process of raising the strength of a weak signal without any change in its general shape is known as **faithful amplification.**

The theory of transistor reveals that it will function properly if its input circuit (*i.e.* base-emitter junction) remains forward biased and output circuit (*i.e.* collector-base junction) remains reverse biased at all times. This is then the key factor for achieving faithful amplification. To ensure this, the following basic conditions must be satisfied :

(*i*) Proper zero signal collector current

(*ii*) Minimum proper base-emitter voltage (V_{BE}) at any instant

(*iii*) Minimum proper collector-emitter voltage (V_{CE}) at any instant

The conditions (*i*) and (*ii*) ensure that base-emitter junction shall remain properly forward biased during all parts of the signal. On the other hand, condition (*iii*) ensures that base-collector junction shall remain properly reverse biased at all times. In other words, the fulfilment of these conditions will ensure that transistor works over the active region of the output characteristics *i.e.* between saturation to cut off.

(*i*) Proper zero signal collector current. Consider an *npn* transistor circuit shown in Fig. 9.1 (*i*). During the positive half-cycle of the signal, base is positive w.r.t. emitter and hence base-emitter junction is forward biased. This will cause a base current and much larger collector current to flow in the circuit. The result is that positive half-cycle of the signal is amplified in the collector as shown. However, during the negative half-cycle of the signal, base-emitter junction is reverse biased and hence no current flows in the circuit. The result is that there is no output due to the negative half-cycle of the signal. Thus we shall get an amplified output of the signal with its negative half-cycles completely cut off which is unfaithful amplification.

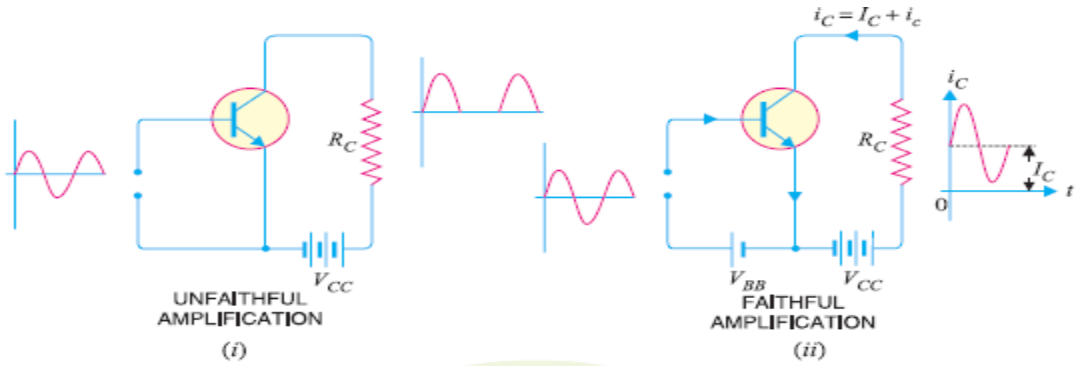

Fig. 9.1

Now, introduce a battery source V_{BB} in the base circuit as shown in Fig. 9.1 (*ii*). The magnitude of this voltage should be such that it keeps the input circuit forward biased even during the peak of negative half-cycle of the signal. When no signal is applied, a d.c. current I_C will flow in the collector circuit due to V_{BB} as shown. This is known as *zero signal collector current* I_C. During the positive half-cycle of the signal, input circuit is more forward biased and hence collector current increases. However, during the negative half-cycle of the signal, the input circuit is less forward biased and collector current decreases. In this way, negative half-cycle of the signal also appears in the output and hence faithful amplification results. It follows, therefore, that for faithful amplification, proper zero signal collector current must flow. *The value of zero signal collector current should be atleast equal to the maximum collector current due to signal alone i.e.*

(ii) Proper minimum base-emitter voltage. In order to achieve faithful amplification, the base-emitter voltage (V_{BE}) should not fall below 0.5V for germanium transistors and 0.7V for *Si* transistors at any instant.

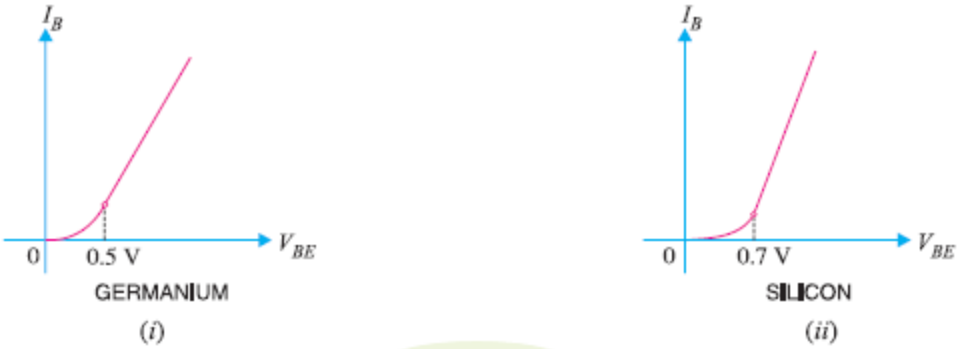

Fig. 9.3

The base current is very small until the *input voltage overcomes the potential barrier at the base-emitter junction. The value of this potential barrier is 0.5V for Ge transistors and 0.7V for *Si* transistors as shown in Fig. 9.3. Once the potential barrier is overcome, the base current and hence collector current increases sharply. Therefore, if base-emitter voltage V_{BE} falls below these values during any part of the signal, that part will be amplified to lesser extent due to small collector current. This will result in unfaithful amplification.

(iii) Proper minimum V_{CE} at any instant. For faithful amplification, the collector-emitter voltage V_{CE} should not fall below 0.5V for Ge transistors and 1V for silicon transistors. This is called *knee voltage* (See Fig. 9.4).

* In practice, a.c. signals have small voltage level (< 0.1V) and if applied directly will not give any collector current.

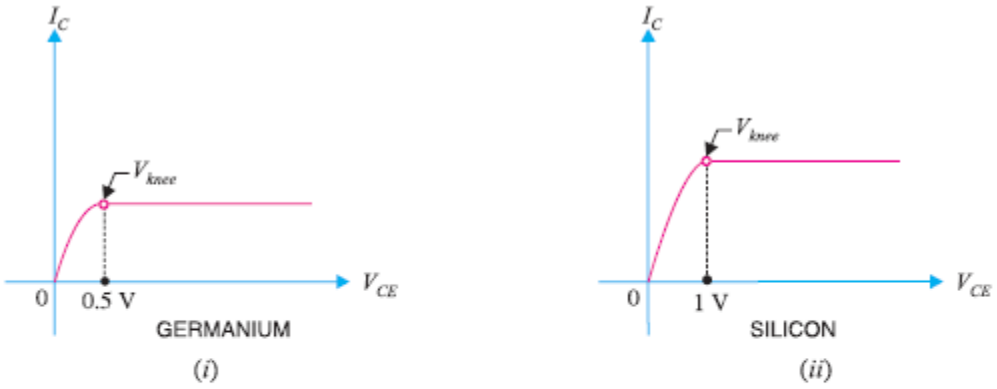

Fig. 9.4

When V_{CE} is too low (less than 0.5V for *Ge* transistors and 1V for *Si* transistors), the collector-base junction is not properly reverse biased. Therefore, the collector cannot attract the charge carriers emitted by the emitter and hence a greater portion of them goes to the base. This decreases the collector current while base current increases. Hence, value of β falls. Therefore, if V_{CE} is allowed to fall below V_{knee} during any part of the signal, that part will be less amplified due to reduced β. This will result in unfaithful amplification. However, when V_{CE} is greater than V_{knee}, the collector-base junction is properly reverse biased and the value of β remains constant, resulting in faithful amplification.

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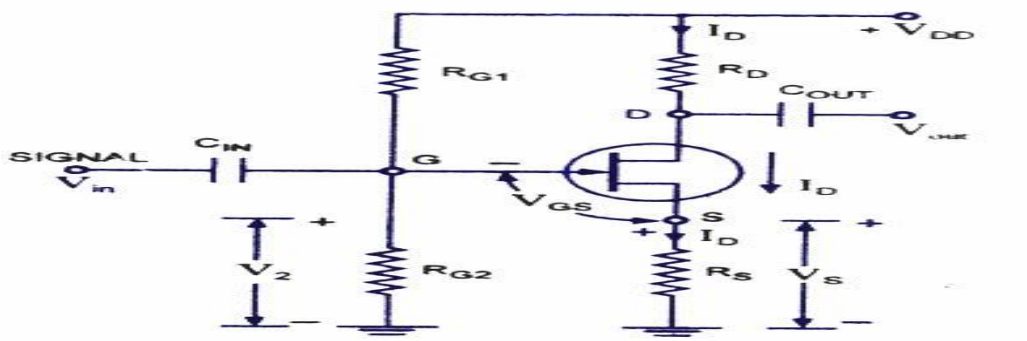


Potential-Divider Bias Circuit For N-Channel JFET

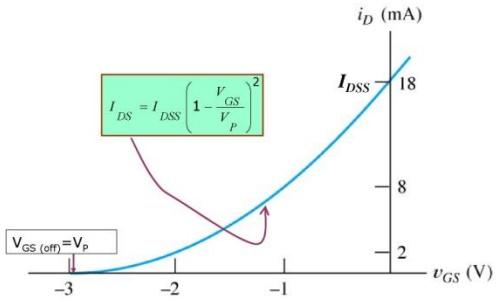
The resistors R_{Gl} and R_{G2}form a potential divider across drain supply V_{DD}. The voltage V_2 across R_{G2} provides the necessary bias.The gate is reverse biased so that $I_G = 0$ and gate voltage is:

$$\mathbf{V_G = V_2 = (V_{DD}/R_{G1} + R_{G2}) * R_{G2} \quad And \quad V_{GS} = V_G - V_S = V_G - I_D R_S}$$

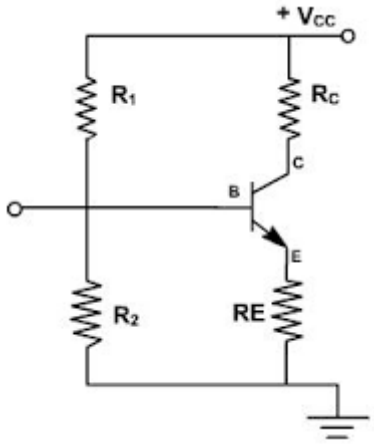
The circuit is so designed that $I_D R_s$ is greater than VG so that VGS is negative. This provides correct bias voltage. The operating point can be determined as:

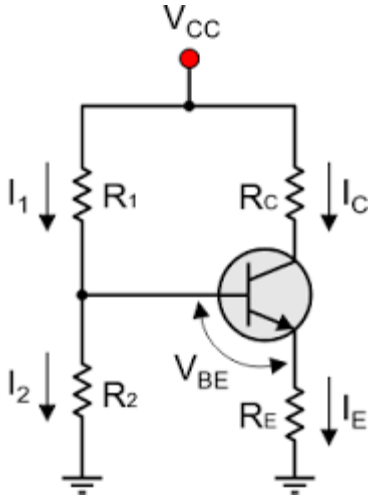
$$\mathbf{I_D = (V_G - V_{GS})/ R_S \quad And \quad V_{DS} = V_{DD} - I_D (R_D + R_S)}$$

TRANSFER CHARACTERISTICS:



Voltage divider bias is the most popular and used way to bias a transistor. It uses a few resistors to make sure that voltage is divided and distributed into the transistor at correct levels. One resistor, the emitter resistor, RE also helps provide stability.



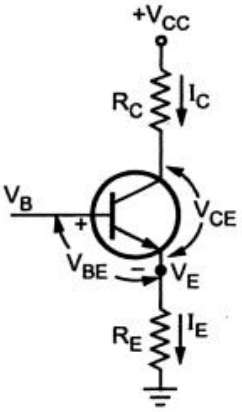


Determining Thevinin Voltage and Resistance:

Collector circuit

Figure 1.31

Divider biased



Now, let us consider the collector circuit as shown in Fig. 1.31.

Voltage across R_E (V_E) can be obtained as,

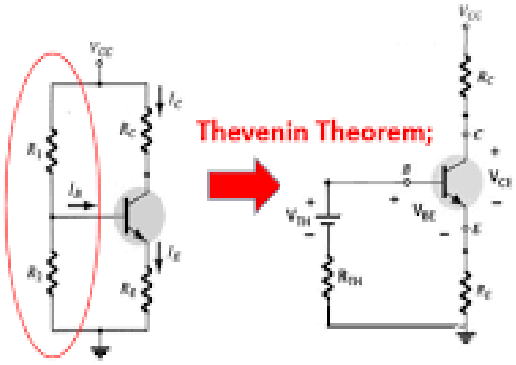
$$V_E = I_E R_E = V_B - V_{BE}$$

$$\therefore \quad I_E = \frac{V_B - V_{BE}}{R_E} \qquad \ldots (11)$$

Applying KVL to the collector circuit we get,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\therefore \quad V_{CE} = V_{CC} - I_C R_C - I_E R_E \qquad \ldots (12)$$



From Thevenin Theorem;

$$R_{TH} = R_1 \,//\, R_2 = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}$$

STABILITY FACTOR – S:

Applying KVL to the base circuit we get,

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

Differentiating w.r.t. I_C and considering V_{BE} to be independent of I_C we get,

$$0 = \frac{\partial I_B}{\partial I_C} \times R_B + \frac{\partial I_B}{\partial I_C} \times R_E + R_E$$

$$\frac{\partial I_B}{\partial I_C}(R_E + R_B) = -R_E$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_E + R_B} \qquad \ldots (15)$$

We have already seen the generalized expression for stability factor S given by

$$S = \frac{1+\beta}{1-\beta\,(\partial I_B / \partial I_C)} \qquad \ldots (16)$$

Substituting value of $\frac{\partial I_B}{\partial I_C}$ in the equation (16) we get,

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E + R_B}\right)} \qquad \ldots (17)$$

$$S = \frac{(1+\beta)(R_E + R_B)}{R_B + R_E + \beta R_E} = \frac{(1+\beta)(R_E + R_B)}{R_B + (1+\beta) R_E}$$

Dividing each term by R_E we get,

$$S = (1+\beta) \frac{1 + R_B/R_E}{(1+\beta) + R_B/R_E} \quad \ldots (18)$$

From equation (16) we can observe following important points

1. The ratio R_B/R_E controls value of stability factor S. If $R_B/R_E << 1$ then equation (18) reduces to

   $$S = (1+\beta) \cdot \frac{1}{(1+\beta)} = 1 \quad \ldots (19)$$

   Practically $R_B/R_E \neq 0$. But to have better stability factor S we have to keep ratio R_B/R_E as small as possible.

2. To keep R_B/R_E small, it is necessary to keep R_B small. This means that $R_1 \,||\, R_2$ must be small. Due to small value of R_1 and R_2, potential divider circuit will draw more current from V_{CC} reducing the life of the battery. So while designing if we make R_2 much smaller than R_1 then parallel combination results small R_B without drawing more current through V_{CC}.

Advantages of the Voltage Divider Bias

1. The resistors help to give complete control over the voltage and current that each region receives in the transistor.
2. And the emitter resistor, RE, allows for stability of the gain of the transistor, despite fluctuations in the β value

The collector current in a transistor changes rapidly when

(*i*) the temperature changes,

(*ii*) the transistor is replaced by another of the same type. This is due to the inherent variations of transistor parameters.

When the temperature changes or the transistor is replaced, the operating point (*i.e.* zero signal I_C and V_{CE}) also changes. However, for faithful amplification, it is essential that operating point remains fixed. This necessitates to make the operating point independent of these variations. This is known as stabilisation.

The process of making operating point independent of temperature changes or variations in transistor parameters is known as **stabilisation.**

Once stabilisation is done, the zero signal I_C and V_{CE} become independent of temperature variations or replacement of transistor *i.e.* the operating point is fixed. A good biasing circuit always ensures the stabilisation of operating point.

Need for stabilisation. Stabilisation of the operating point is necessary due to the following reasons :

(*i*) Temperature dependence of I_C

(*ii*) Individual variations

(*iii*) Thermal runaway

(*i*) **Temperature dependence of I_C.** The collector current I_C for CE circuit is given by:

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta + 1) I_{CBO}$$

The collector leakage current I_{CBO} is greatly influenced (especially in germanium transistor) by temperature changes. A rise of 10°C doubles the collector leakage current which may be as high as 0.2 mA for low powered germanium transistors. As biasing conditions in such transistors are generally so set that zero signal I_C = 1mA, therefore, the change in I_C due to temperature variations cannot be tolerated. This necessitates to stabilise the operating point *i.e.* to hold I_C constant inspite of temperature variations.

(*ii*) **Individual variations.** The value of β and V_{BE} are not exactly the same for any two transistors even of the same type. Further, V_{BE} itself decreases when temperature increases. When a transistor is replaced by another of the same type, these variations change the operating point. This necessitates to stabilise the operating point *i.e.* to hold I_C constant irrespective of individual variations in transistor parameters.

(*iii*) **Thermal runaway.** The collector current for a *CE* configuration is given by :

$$I_C = \beta I_B + (\beta + 1) I_{CBO} \qquad (i)$$

The collector leakage current I_{CBO} is strongly dependent on temperature. The flow of collector current produces heat within the transistor. This raises the transistor temperature and if no stabilisation is done, the collector leakage current I_{CBO} also increases. It is clear from exp. (*i*) that if I_{CBO} increases, the collector current I_C increases by $(\beta + 1)\, I_{CBO}$. The increased I_C will raise the temperature of the transistor, which in turn will cause I_{CBO} to increase. This effect is cumulative and in a matter of seconds, the collector current may become very large, causing the transistor to burn out.

The self-destruction of an unstabilised transistor is known as **thermal runaway.**

In order to avoid thermal runaway and consequent destruction of transistor, it is very essential that operating point is stabilised *i.e.* I_C is kept constant. In practice, this is done by causing I_B to decrease automatically with temperature increase by circuit modification. Then decrease in βI_B will compensate for the increase in $(\beta + 1)\, I_{CBO}$, keeping I_C nearly constant. In fact, this is what is always aimed at while building and designing a biasing circuit.

9.5 Essentials of a Transistor Biasing Circuit

It has already been discussed that transistor biasing is required for faithful amplification. The biasing network associated with the transistor should meet the following requirements :

(*i*) It should ensure proper zero signal collector current.

(*ii*) It should ensure that V_{CE} does not fall below 0.5 V for *Ge* transistors and 1 V for silicon transistors at any instant.

(*iii*) It should ensure the stabilisation of operating point.

It has already been discussed that transistor biasing is required for faithful amplification. The biasing network associated with the transistor should meet the following requirements :

(*i*) It should ensure proper zero signal collector current.

(*ii*) It should ensure that V_{CE} does not fall below 0.5 V for *Ge* transistors and 1 V for silicon transistors at any instant.

(*iii*) It should ensure the stabilisation of operating point.

9.6 Stability Factor

It is desirable and necessary to keep I_C constant in the face of variations of I_{CBO} (sometimes represented as I_{CO}). The extent to which a biasing circuit is successful in achieving this goal is measured by stability factor S. It is defined as under :

The rate of change of collector current I_C w.r.t. the collector leakage current $^*I_{CO}$ *at constant β and I_B is called* **stability factor** *i.e.*

$$\text{Stability factor, } S = \frac{dI_C}{dI_{CO}} \text{ at constant } I_B \text{ and } \beta$$

The stability factor indicates the change in collector current I_C due to the change in collector leakage current I_{CO}. Thus a stability factor 50 of a circuit means that I_C changes 50 times as much as any change in I_{CO}. In order to achieve greater thermal stability, it is desirable to have as low stability factor as possible. The ideal value of S is 1 but it is never possible to achieve it in practice. Experience shows that values of S exceeding 25 result in unsatisfactory performance.

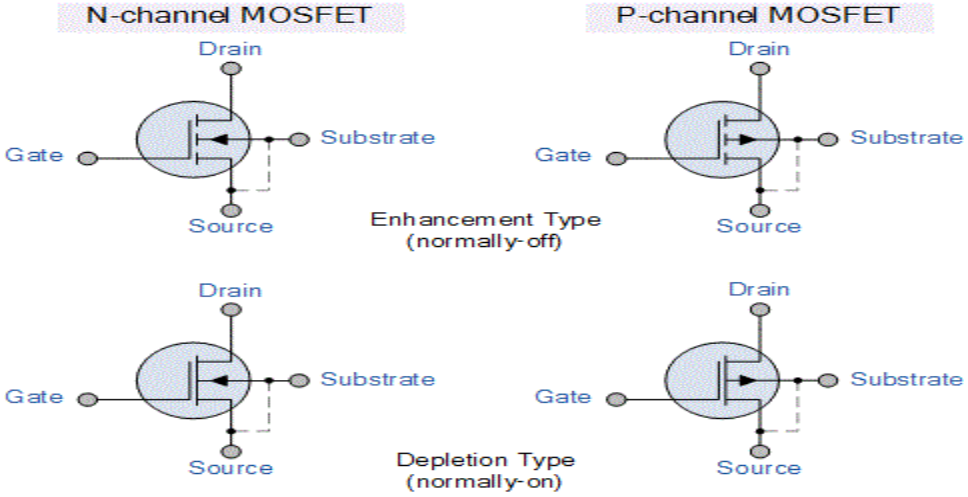
The general expression of stability factor for a C.E. configuration can be obtained as under:

$$I_C = \beta I_B + (\beta + 1)\, I_{CO}$$

** Differentiating above expression *w.r.t.* I_C, we get,

The metal–oxide–semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET) is a type of transistor used for amplifying or switching electronic signals.Although the MOSFET is a four-terminal device with source (S), gate (G), drain (D), and body (B) terminals,the body (or substrate) of the MOSFET is often connected to the source terminal, making it a three-terminal device like other field-effect transistors.The main advantage of a MOSFET over a regular transistor is that it requires very little current to turn on (less than 1mA), while delivering a much higher current to a load.
The main difference this time is that MOSFETs are available in two basic forms:

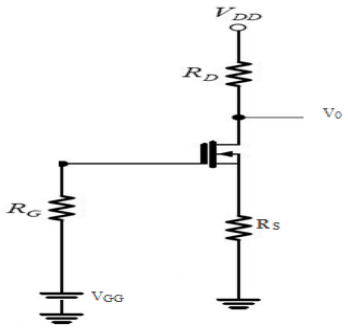
1. **Depletion Type** – the transistor requires the Gate-Source voltage, (V_{GS}) to switch the device "OFF". The depletion mode MOSFET is equivalent to a "Normally Closed" switch.
2. **Enhancement Type** – the transistor requires a Gate-Source voltage, (V_{GS}) to switch the device "ON". The enhancement mode MOSFET is equivalent to a "Normally Open" switch.



Common FET Biasing Circuits

- Fixed – Bias
- Self-Bias
- Voltage-Divider Bias

Fixed – Bias



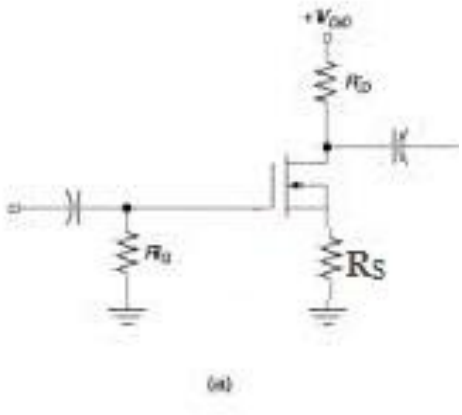
For all FETs:

$$I_G \approx 0A \qquad I_D = I_S \qquad I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$V_D = V_{DS}$ $V_G = V_{GS}$

It is called *fixed-bias configuration* due to V_{GG} is a fixed power supply so V_{GS} is fixed

Self-Bias



Since no gate current flows through the reverse-biased gate-source, the gate current $I_G = 0$ and, therefore,

$$V_G = I_G R_G = 0$$

With a drain current I_D the voltage at the S is

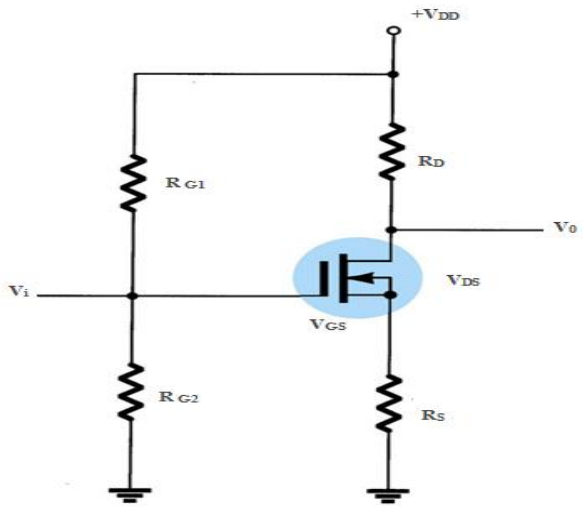
$V_S = I_S R_S$ AND $I_S = I_D$

The gate-source voltage is then

$V_{GS} = V_G - V_S = 0 - I_D R_S = - I_D R_S$

So voltage drop across resistance R_S provides the biasing voltage V_{GS} and no external source is required for biasing and this is the reason that it is called self-biasing.

Voltage-Divider Bias



The resistors R_{Gl} and R_{G2}form a potential divider across drain supply V_{DD}. The voltage V_2 across R_{G2} provides the necessary bias.The gate is reverse biased so that $I_G = 0$ and gate voltage is:

$$V_G = V_2 = (V_{DD}/R_{G1+}R_{G2}) * R_{G2} \quad \text{And} \quad V_{GS} = V_G - V_S = V_G - I_D R_S$$

The circuit is so designed that $I_D R_s$ is greater than VG so that VGS is negative. This provides correct bias voltage. The operating point can be determined as:

$$I_D = (V_G - V_{GS})/ R_S \quad \text{And} \quad V_{DS} = V_{DD} - I_D (R_D + R_S)$$

When only one transistor with associated circuitry is used for amplifying a weak signal, the circuit is known as **single stage transistor amplifier.**

A single stage transistor amplifier has one transistor, bias circuit and other auxiliary components. Although a practical amplifier consists of a number of stages, yet such a complex circuit can be conveniently split up into separate single stages. By analysing carefully only a single stage and using this single stage analysis repeatedly, we can effectively analyse the complex circuit. It follows, therefore, that single stage amplifier analysis is of great value in understanding the practical amplifier circuits.

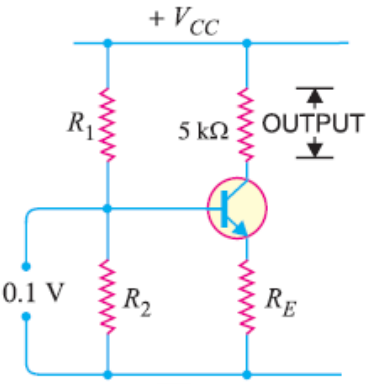
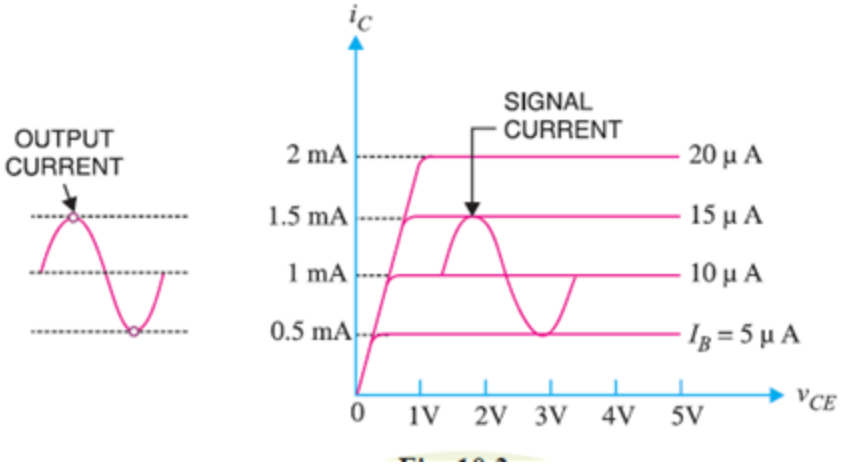


Fig. 10.1

Fig. 10.1 shows a single stage transistor amplifier. When a weak a.c. signal is given to the base of transistor, a small base current (which is a.c.) starts flowing. Due to transistor action, a much larger (β times the base current) a.c. current flows through the collector load R_C. As the value of R_C is quite high (usually 4-10 kΩ), therefore, a large voltage appears across R_C. Thus, a weak signal applied in the base circuit appears in amplified form in the collector circuit. It is in this way that a transistor acts as an amplifier.

The action of transistor amplifier can be beautifully explained by referring to Fig. 10.1. Suppose a change of 0.1V in signal voltage produces a change of 2 mA in the collector current. Obviously, a signal of only 0.1V applied to the base will give an output voltage = 2 mA × 5 kΩ = 10V. Thus, the transistor has been able to raise the voltage level of the signal from 0.1V to 10V *i.e.* voltage amplification or stage gain is 100.

The function of transistor as an amplifier can also be explained graphically. Fig. 10.2 shows the output characteristics of a transistor in *CE* configuration. Suppose the zero signal base current is 10 μA *i.e.* this is the base current for which the transistor is biased by the biasing network. When an a.c. signal is applied to the base, it makes the base, say positive in the first half-cycle and negative in the second half-cycle. Therefore, the base and collector currents will increase in the first half-cycle when base-emitter junction is more forward-biased. However, they will decrease in the second half-cycle when the base-emitter junction is less forward biased.



Practical circuit of Transistor Amplifier

It is important to note that a transistor can accomplish faithful amplification only if proper associated circuitry is used with it. Fig. 10.3 shows a practical single stage transistor amplifier. The various circuit elements and their functions are described below :

***(i)* Biasing circuit.** The resistances R_1, R_2 and R_E form the biasing and stabilisation circuit. The biasing circuit must establish a proper operating point otherwise a part of the negative half-cycle of the signal may be cut off in the output.

***(ii)* Input capacitor C_{in}.** An electrolytic capacitor C_{in} ($\simeq 10$ μF) is used to couple the signal to the base of the transistor. If it is not used, the signal source resistance will come across R_2 and thus change the bias. The capacitor C_{in} allows only a.c. signal to flow but isolates the signal source from R_2.*

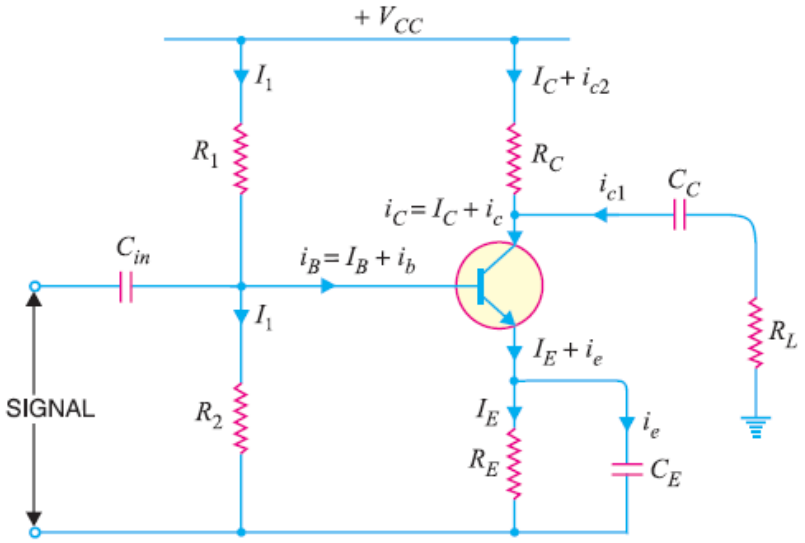


Fig. 10.3

(iii) Emitter bypass capacitor C_E. An emitter bypass capacitor C_E ($\simeq 100\mu F$) is used in parallel with R_E to provide a low reactance path to the amplified a.c. signal. If it is not used, then amplified a.c. signal flowing through R_E will cause a voltage drop across it, thereby reducing the output voltage.

(iv) Coupling capacitor C_C. The coupling capacitor C_C ($\simeq 10\mu F$) couples one stage of ampli-

Various circuit currents. It is useful to mention the various currents in the complete amplifier circuit. These are shown in the circuit of Fig. 10.3.

(i) Base current. When no signal is applied in the base circuit, d.c. base current I_B flows due to biasing circuit. When a.c. signal is applied, a.c. base current i_b also flows. Therefore, with the application of signal, total base current i_B is given by:

$$i_B = I_B + i_b$$

(ii) Collector current. When no signal is applied, a d.c. collector current I_C flows due to biasing circuit. When a.c. signal is applied, a.c. collector current i_c also flows. Therefore, the total collector current i_C is given by:

$$i_C = I_C + i_c$$

where

$$I_C = \beta I_B = \text{zero signal collector current}$$

$$i_c = \beta i_b = \text{collector current due to signal.}$$

(iii) Emitter current. When no signal is applied, a d.c. emitter current I_E flows. With the application of signal, total emitter current i_E is given by :

$$i_E = I_E + i_e$$

It is useful to keep in mind that :

$$I_E = I_B + I_C$$

$$i_e = i_b + i_c$$

Now base current is usually very small, therefore, as a reasonable approximation,

$$I_E \simeq I_C \quad \text{and} \quad i_e \simeq i_c$$

AC Analysis

The Common-Emitter Amplifier is used to achieve high voltage gain and employs a bi-junction transistor (BJT).

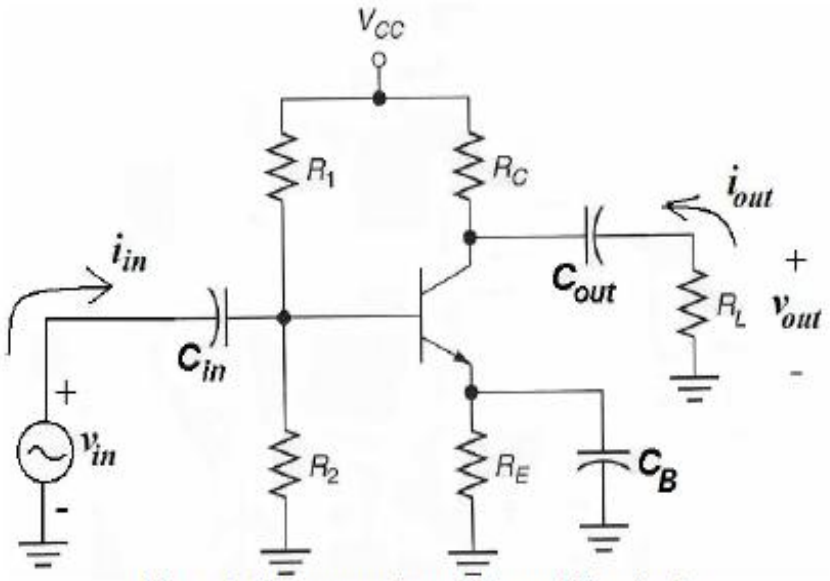


Figure 1. Common emitter (CE) amplifier circuit

- The AC voltage V*in* is provided by an audio source such as a microphone or an MP3 player.
- The resistance RL is the load resistance or could be the resistance of an audio speaker.
- One purpose of Cin is to prevent DC current from flowing from Vcc to *Vin*, and thus preventing damage to the audio source.
- The purpose of Cout is to prevent DC current flowing from Vcc to *Vout*. This will prevent damage to the audio speaker or it will prevent DC loading effects on the next amplifier stage.

Compute the voltage gain $A_v = \frac{v_{out}}{v_{in}}$

The AC resistance of the base-emitter junction (rbe) is calculated from:

By Ohm's law, the AC base current is $i_b = \frac{v_{in}}{r_{be}}$ (2)

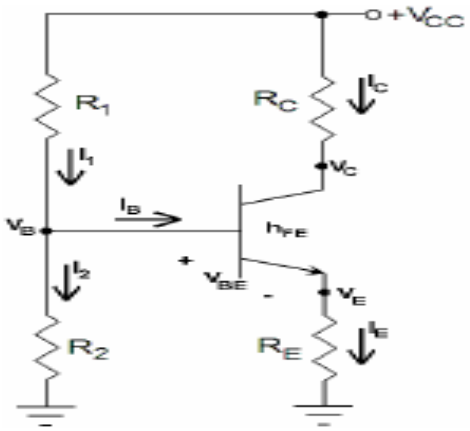
The AC collector current is $i_c = h_{fe} i_b$ (3)

The AC collector current is pulled through the parallel combination of R_C and R_L. So by Ohm's Law, the output voltage is:

$$v_{out} = i_c (R_C \| R_L) \quad (4)$$

DC Analysis

For DC analysis, we can remove all capacitors, since there is no DC current through them. The DC equivalent circuit is shown below.



DC equivalent circuit of a common emitter amplifier

About transistor amplifiers: When a transistor is operating as an amplifier, the DC current gain (hFE) is a given constant value. The typical values for hFE range from 75 to 200, depending on the type of BJT. The resistors R1 and R2 form a voltage divider to provide a stable base voltage.

By Ohm's law, the emitter voltage is $V_E = I_E R_E$ (1)

By KVL, the base voltage is $V_B = V_{BE} + V_E$ (2)

Substituting (2) into (1) gives us $V_B = V_{BE} + I_E R_E$ (3)

Let's assume the transistor is operating correctly with a base-emitter voltage (V_{BE}) is about 0.7 volts. Therefore, the base voltage is:

$$V_B = 0.7 + I_E R_E \quad (4)$$

The transistor currents obey KCL:

$$I_E = I_B + I_C \quad (5)$$

Substituting $I_C = h_{FE} I_B$ into (5) gives us

$$\begin{aligned} I_E &= I_B + h_{FE} I_B \\ &= I_B (h_{FE} + 1) \end{aligned} \quad (6)$$

Substituting (6) into (4) yields

$$\begin{aligned} V_B &= 0.7 + V_E \\ &= 0.7 + I_B (h_{FE} + 1) R_E \end{aligned} \quad (7)$$

Ohm's law for the base voltage through resistor R_2 is:

$$V_B = I_2 R_2 \quad (8)$$

Equating (7) with (8) yields

$$I_2 R_2 = 0.7 + I_B (h_{FE} + 1) R_E \quad (9)$$

By KCL, the base current can be expressed as:

$$I_B = I_1 - I_2 \quad (10)$$

Substituting (11) into (10), yields

$$I_2 R_2 = 0.7 + (I_1 - I_2)(h_{FE} + 1) R_E \quad (11)$$

We can arrange (11) into the form, $aI_1 + bI_2 = c$, as follows:

$$\begin{aligned} I_2R_2 &= 0.7 + (I_1 - I_2)(h_{FE}+1)R_E \\ &= 0.7 + (I_1)(h_{FE}+1)R_E - (I_2)(h_{FE}+1)R_E \end{aligned} \tag{12}$$

Group current terms of the left side to obtain

$$-I_1(h_{FE}+1)R_E + I_2R_2 + I_2(h_{FE}+1)R_E = 0.7 \tag{13}$$

Simplify left side to obtain

$$-I_1(h_{FE}+1)R_E + I_2\left(R_2 + (h_{FE}+1)R_E\right) = 0.7 \tag{14}$$

KVL from V_{CC} through R_1 and R_2 yields

$$I_1R_1 + I_2R_2 = V_{CC} \tag{15}$$

Equations (14) and (15) form a system of two equations and two unknowns (I_1 and I_2). These can be formed into a matrix equation:

$$\begin{bmatrix} -(h_{FE}+1)R_E & R_2 + (h_{FE}+1)R_E \\ R_1 & R_2 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0.7 \\ V_{CC} \end{bmatrix} \tag{16}$$

The matrix equation can be solved by inverting the resistance matrix:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} -(h_{FE}+1)R_E & R_2 + (h_{FE}+1)R_E \\ R_1 & R_2 \end{bmatrix}^{-1} \begin{bmatrix} 0.7 \\ V_{CC} \end{bmatrix}$$

.

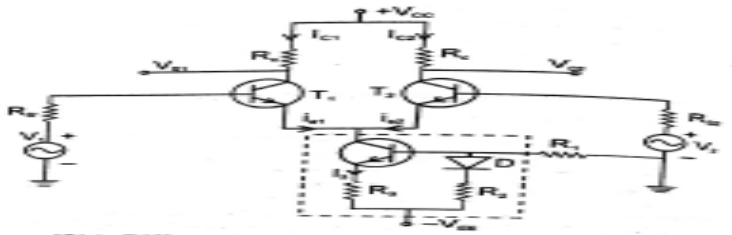


Figure 45(a) Differential amplifier with constant current source

$R_E = R_e$ of $Q_3 = \frac{1}{h_{oe}} \cdot (R_1 + h_{ie}) \left[1 + \frac{1}{h_{oe} R_1}\right]$ = output impedance of Q_3 is

(In the approximate model, $h_{ob} = 0$, $R_E = \infty$) practically R_e will be in hundred of kilo ohms even if R_3 is small.

It is further seen that the transistor Q_3 shown in the circuit acts as a constant current source, it can be proved as follows, assuming that the base current of Q_3 is negligible.

Applying KVL to the base circuit of Q_3.

$$V_{BE3} + I_3R_3 = V_D + \frac{(V_{EE} - V_D)}{R_1 + R_2} \cdot R_2$$

where V_D = diode voltage hence,

$$I_e = I_3 = \frac{1}{R_3}\left\{\frac{V_{EE}R_2}{R_1 + R_2} + \frac{V_DR_1}{R_1 + R_2} - V_{BE3}\right\}$$

$$\frac{V_D R_1}{R_1 + R_2} = V_{BE_3} \quad (34)$$

$$I_o = \frac{V_{EE} R_2}{R_3 (R_1 + R_2)} \quad (35)$$

Since this current is independent of supply voltages V_{s1} and V_{s2}, Q_3 acts to apply constant current I_0 to the differential amplifier consisting of Q_1 and Q_2.

I_o is also independent of temperature because of the diode D. Without diode, the current will vary with temperature because V_{BE_3} decreases approximately 2.5m per °C. The diode has the same temperature dependence and hence the two variation cancel each other and I_o does not vary with temperature.

Since the cut in voltage of diode (V_D) is approximately the same value as the base to emitter voltage V_{be3} of transistor, then equation (28) cannot be satisfied with a single diode. Hence two diodes in series are used for V_D.

Small Signal Operation

The small signal equivalent circuit for the amplifier is exactly identical to that of differential configuration. The important difference between the two transistor amplifier and three transister amplifier is shown in figure 31(a) is the value of R_e is using BJT as a constant current source $R_e \simeq \frac{1}{h_{ob}}$, which is much larger than value of R_e. This leads to much larger CMRR.

Case (I) When common mode input is applied. i.e., $V_d = 0$, and $V_1 = V_2$. As a result of symmetry $I_{e1} = I_{e2}$. The figure 45 (b) can be redrawn as shown in figure 45(c)

Apply KVL to right side circuit.

$$I_{e1} = \frac{V_a}{\frac{R_b}{h_{fe}+1} + h_{ib} + \frac{2}{h_{ob}}} = I_{e2} \quad (36)$$

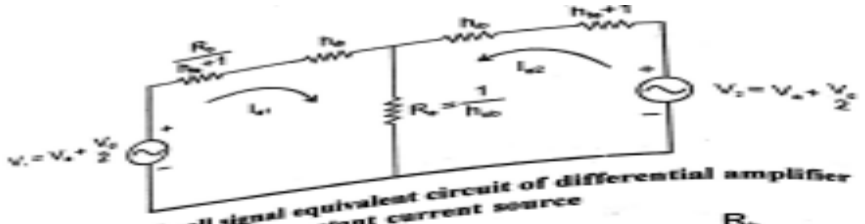


Figure 45(b) Small signal equivalent circuit of differential amplifier with constant current source

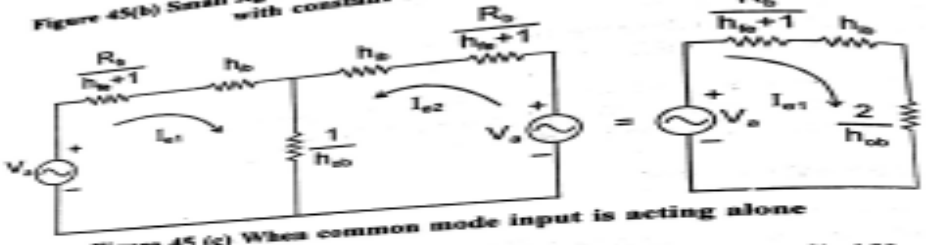


Figure 45 (c) When common mode input is acting alone

Case (II) If set $V_a = 0$ i.e., when differential mode voltage is applied $V_1 = -V_2$ or $I_{e1} = -I_{e2}$. The figure 31(b) can be redrawn as shown in figure (d)

Apply KVL to the right side circuit

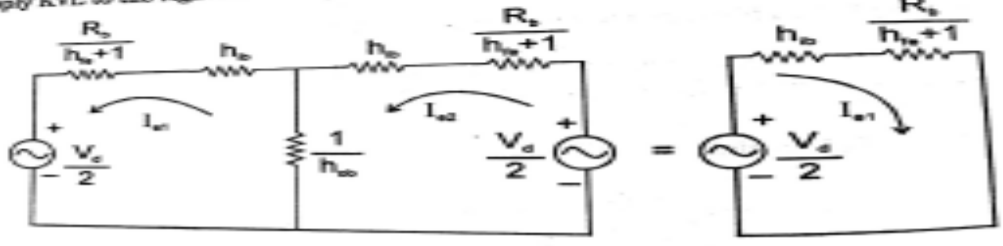


Figure 45(d) When differential mode input is acting alone

hence $$CMRR = \frac{A_d}{A_c} = \frac{\frac{2}{h_{ob}} + h_{ib} + \frac{R_b}{h_{fe}+1}}{2\left(h_{ib} + \frac{R_b}{h_{fe}+1}\right)}$$

The above equation concludes the constant current source increases the CMRR.

Input and Output Resistances of Differential Amplifier

Differential Mode output resistance, $R_{OD} = R_C$

Differential Mode input resistance, $R_{ID} = 2h_{ie}$

Proof is the remains the same given in the previous article.

[It is the resistance measured between the base terminal of Q_1 and Q_2]

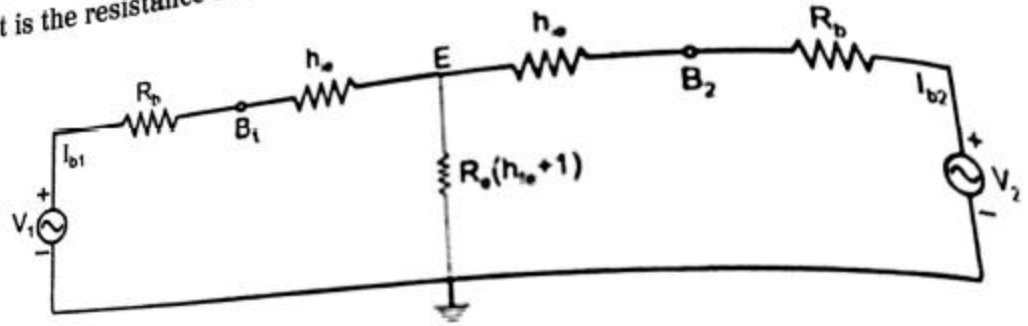


Figure 46 Small Signal Equivalent Circuit of Differential amplifie with constant current Source

Differential amplifier

Fig. 2.95 Emitter biased circuits

The two transistors Q_1 and Q_2 have exactly matched characteristics. The two collector resistances R_{C1} and R_{C2} are equal while the two emitter resistances R_{E1} and R_{E2} are also equal.

Thus $R_{C1} = R_{C2}$ **and** $R_{E1} = R_{E2}$

The magnitudes of $+V_{CC}$ and $-V_{EE}$ are also same. The differential amplifier can be obtained by using such two emitter biased circuits. This is achieved by connecting

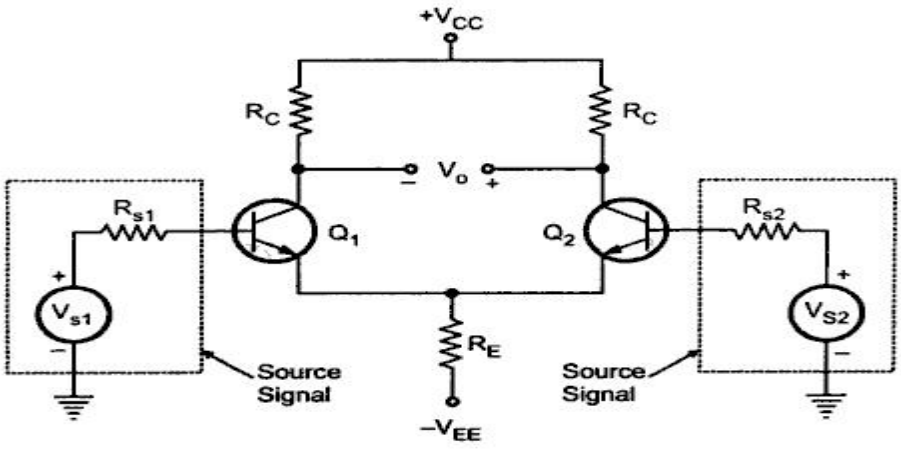
emitter E_1 of Q_1 to the emitter E_2 of Q_2. Due to this, R_{E1} appears in parallel with R_{E2} and the combination can be replaced by a single resistance denoted as R_E. The base B_1 of Q_1 is connected to the input 1 which is V_{S1} while the base B_2 of Q_2 is connected to the input 2 which is V_{S2}. The supply voltages are measured with respect to ground. The balanced output is taken between the collector C_1 of Q_1 and the collector C_2 of Q_2. Such an amplifier is called **emitter coupled differential amplifier**. The two collector resistances are same hence can be denoted as R_C. The complete circuit diagram of such a basic dual input, balanced output differential amplifier

As the output is taken between two output terminals, none of them is grounded, it is called balanced output differential amplifier.

Let us study the circuit operation in the two modes namely

i) Differential mode operation

ii) Common mode operation.



Differential Mode Amplifier:

In the differential mode, the two input signals are different from each other. Consider the two input signals which are same in magnitude but 180° out of phase. These signals, with opposite phase can be obtained from the center tap transformer. The circuit used in differential mode operation is shown in the Fig. 2.97.

Assume that the sine wave on the base of Q_1 is positive going while on the base of Q_2 is negative going. With a positive going signal on the base of Q_1, an amplified negative going signal develops on the collector of Q_1. Due to positive going signal, current through R_E also increases and hence a positive going wave is developed

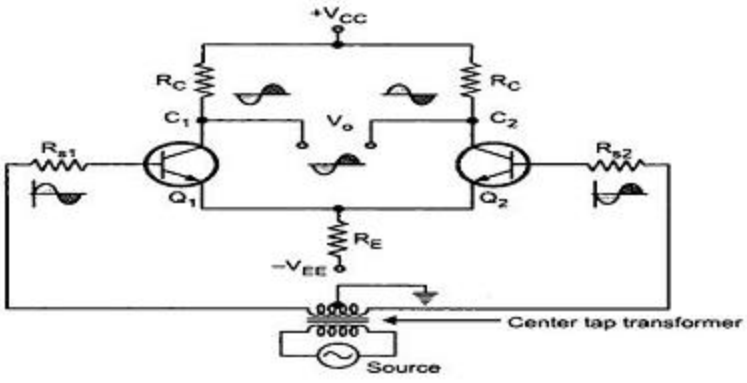


Fig. 2.97 Differential mode operation

across R_E. Due to negative going signal on the base of Q_2, an amplified positive going signal develops on the collector of Q_2. And a negative going signal develops across R_E, because of emitter follower action of Q_2.

So signal voltages across R_E, due to the effect of Q_1 and Q_2 are equal in magnitude and 180° out of phase, due to matched pair of transistors. Hence these two signals cancel each other and there is no signal

While V_o is the output taken across collector of Q_1 and collector of Q_2. The two outputs on collector 1 and 2 are equal in magnitude but opposite in polarity. And V_o is the difference between these two signals, e.g. +10 − (−10) = + 20. Hence the difference output V_o is twice as large as the signal voltage from either collector to ground.

Common Mode Amplifier:

In this mode, the signals applied to the base of Q_1 and Q_2 are derived from the same source. So the two signals are equal in magnitude as well as in phase. The circuit diagram is shown in the Fig. 2.98.

In phase signal voltages at the bases of Q_1 and Q_2 causes in phase signal voltages to appear across R_E, which add together. Hence R_E carries a signal current and provides a negative feedback. This feedback reduces the common mode gain of differential amplifier.

While the two signals causes in phase signal voltages of equal magnitude to appear across the two collectors of Q_1 and Q_2. Now the output voltage is the difference between the two collector voltages, which are equal and also same in phase, e.g. (10) − (10) = 0. Thus the difference output V_o is almost zero, negligibly small. **Ideally it should be zero.**

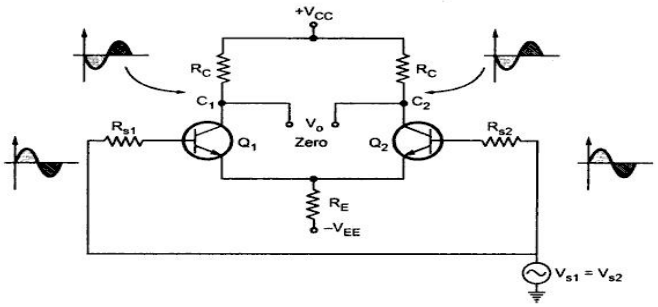


Fig. 2.98 Common mode operation

(a) Darlington Emitter Follower

The Darlington transistor (often called a Darlington pair) is a compound structure consisting of two bipolar transistors connected in such a way that the current amplified by the first transistor is amplified further by the second one.

A Darlington pair behaves like a single transistor with a high current gain

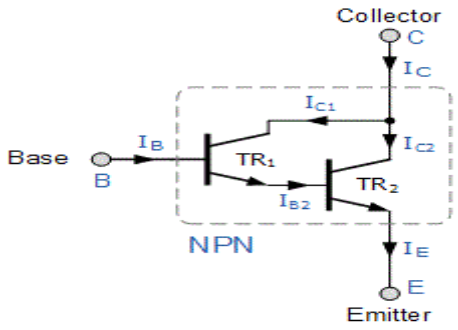
A general relation between the compound current gain and the individual gains is given by:

$$\beta_{\text{Darlington}} = \beta_1 \cdot \beta_2 + \beta_1 + \beta_2$$

If β_1 and β_2 are high enough (hundreds), this relation can be approximated with:

$$\beta_{\text{Darlington}} \approx \beta_1 \cdot \beta_2$$

A darlington emitter follower is two transistors operating as one. Both collectors are tied together. The emitter of the first is connected to the base of the second.



A Darlington Transistor configuration, also known as a "Darlington pair" or "super-alpha circuit", consist of two NPN or PNP transistors connected together so that the emitter current of the first transistor TR1 becomes the base current of the second transistor TR2. Then transistor TR1 is connected as an emitter follower and TR2 as a common emitter amplifier

$$I_C = I_{C1} + I_{C2}$$
$$I_C = \beta_1.I_B + \beta_2.I_{B2}$$

But the base current, I_{B2} is equal to transistor TR1 emitter current, I_{E1} as the emitter of TR1 is connected to the base of TR2. Therefore:

$$I_{B2} = I_{E1} = I_{C1} + I_B = \beta_1.I_B + I_B = (\beta_1 + 1).I_B$$

Then substituting in the first equation:

$$I_C = \beta_1.I_B + \beta_2.(\beta_1 + 1).I_B$$

$$I_C = \beta_1.I_B + \beta_2.\beta_1.I_B + \beta_2.I_B$$

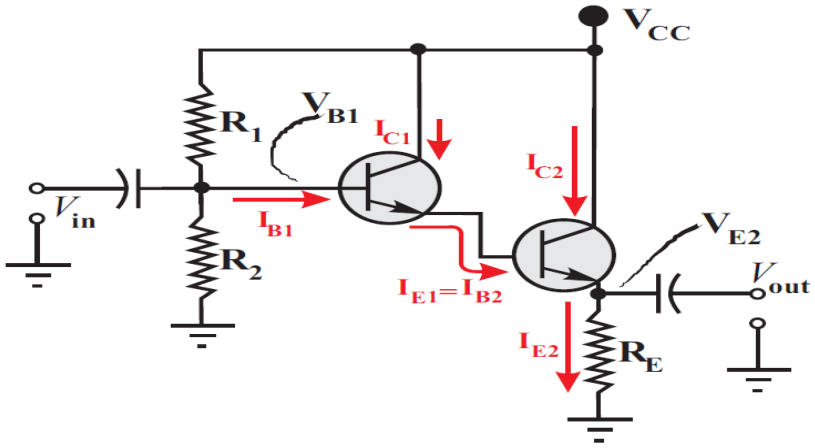
$$I_C = (\beta_1 + (\beta_2.\beta_1) + \beta_2).I_B$$

Where β_1 and β_2 are the gains of the individual transistors.

This means that the overall current gain, β is given by the gain of the first transistor multiplied by the gain of the second transistor. In other words, a pair of bipolar transistors

combined together to make a single Darlington transistor pair can be regarded as a single transistor with a very high value of β and consequently a high input resistance.

Operation of Darlington Emitter Follower



This is a special case emitter follower that uses two transistors to increase the overall values of circuit current gain (A) and input impedance (Z).

The emitter of the first transistor is tied to the base of the second. The collector terminals are tied together.

AC ANALYSIS

The ac current gain of the Darlington pair is the product of the individual gains. This can easily be in the thousands. Even with the losses associated with the input and output circuits , the overall current gain of Darlington amplifier is very high. Even though the Darlington amplifier has a high current gain, the voltage gain (A) is slightly less than 1.

DC ANALYSIS

VBE= VB1 - VE2
VE2 = VB1 - 1.4 V
VB1= R2/ (R1+ R2) VCC
IE2= VE2 / RE

Disadvantages:

One drawback is an approximate doubling of the base/emitter voltage. Since there are two junctions between the base and emitter of the Darlington transistor, the equivalent base/emitter voltage is the sum of both base/emitter voltages:

$$V_{BE} = V_{BE1} + V_{BE2} \approx 2V_{BE1}$$

For silicon-based technology, where each V_{BE} is about 0.7 V when the device is operating in the active or saturated region, the necessary base/emitter voltage of the pair is 1.4 V.

(b) Bootstrap Darlington Emitter Follower

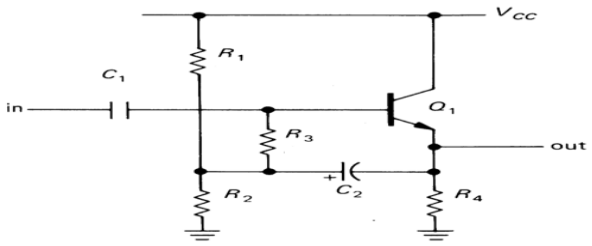
A bootstrap circuit is one where part of the output of an amplifier stage is applied to the input, so as to alter the input impedance of the amplifier. When applied deliberately, the intention is usually to increase rather than decrease the impedance.

In the domain of MOSFET circuits, "bootstrapping" is commonly used to mean pulling up the operating point of a transistor above the power supply.

Bootstrapping (Using positive feedback to feed part of the output back to the input, but without causing oscillation) is a method of apparently increasing the value of a fixed resistor as it appears to A.C. signals, and thereby increasing input impedance. The capacitor Co is the 'Bootstrap Capacitor', which provides A.C. feedback to a resistor in series with the base.

"Bootstrapping" increases Zin at signal frequencies without disturbing the DC bias

BOOTSTRAPPING EMITTER FOLLOWER



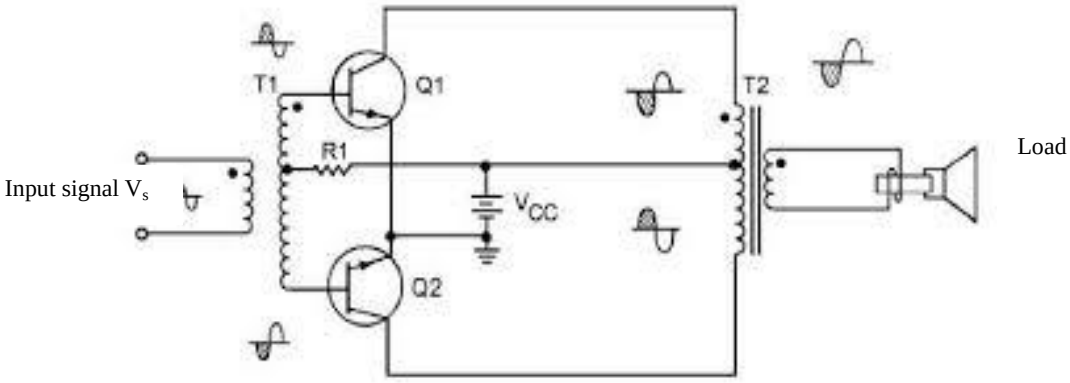
The relatively low input impedance of the circuit can be increased significantly by *bootstrapping* . The resistor R3 is located between the R1-R2 junction and the base of transistor Q1, and the input signal is fed to Q1's base through capacitor C1. To make this point clearer, consider that the emitter-follower circuit has a precise voltage gain of unity. In this condition, identical signal voltages would appear at the two ends of R3, so no signal current would flow in this resistor, making it "appear" equal to R_{in} .We have,

Ri=Vi/Ii =hfe1.hfe2.RC

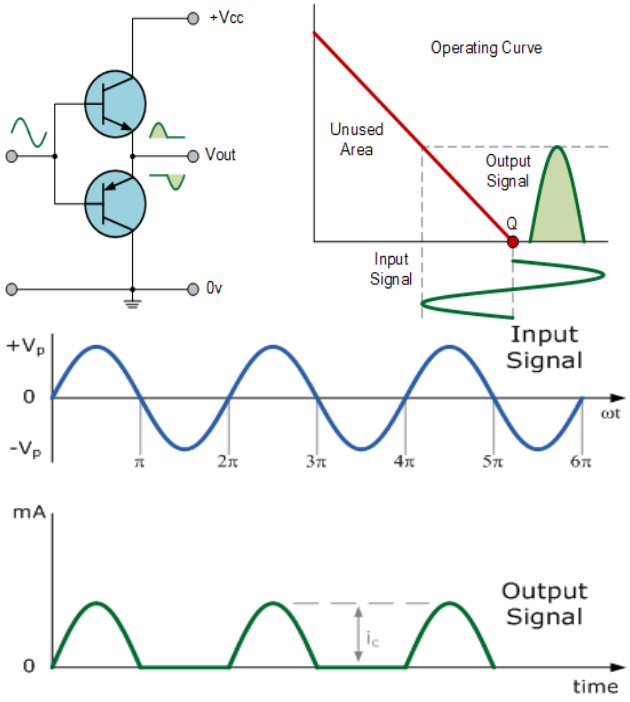
UNIT III

Class B amplifiers were invented as a solution to the efficiency and heating problems associated with the previous class A amplifier. The basic class B amplifier is designed with its output stage configured in a "push-pull" type arrangement, so that each transistor device amplifies only half of the output waveform.

Transformer Coupled Push-Pull Class-B Amplifier



Class B Output Waveform



Operation:

a) The transistors of both p-n-p and n-p-n can be used.
b) Push pull amplifier shown fig a use n-p-n and p-n-p transistor

c) The circuits consist of two centre tapped transformer
d) The transformer on the I/P side is known as driver transformer & the other on the load side is known as O/P transformer.
e) The I/P signal 'Vs' is applied to the primary winding of the i/p transformer.

The operation of the circuit can be divided into two parts:

1) Operation in the positive half cycle of i/p:

a) In the positive half cycle of i/p, secondary voltage of the driver transformer, 'A' is positive & 'B' is negative.
b) Base- Emitter junction of transistor Q1 is forward bias & Base- Emitter junction of Q2 is Reverse Bias. i.e. Q1 conducts & Q2 turn off
c) Thus base current for Q1 i.e.,I_{b1}, will flow & I_{b2} =o
d) Hence the collector current I.e. I_{C1} will flow & I_{C2}=0
e) A positive sinusoidal voltage will appear across the load

2) Operation in the negative half cycle of i/p:-

a) In the negative half cycle of i/p 'A' is negative & 'B" is positive
b) Base- Emitter junction of transistor Q1 is Reverse Bias. & Base- Emitter junction of transistor Q2 is forward bias
c) The base current I_{b1}= 0 & I_{b2} will flow through transistor Q2
d) Thus in this half cycle Q1 is OFF & Q2 is ON
e) Hence the collector current i.e. I_{C2} flows through the output transformer & I_{C1} =0
f) Hence a negative sinusoidal voltage will appear across the load.

Thus at a time only one transistor will conduct.

Result:

Then we can see that each transistor device of the class B amplifier only conducts through one half or 180 degrees of the output waveform in strict time alternation, but as the output stage has devices for both halves of the signal waveform the two halves are combined together to produce the full linear output waveform.

Demerits:

This push-pull design of amplifier is obviously more efficient than Class A, but the problem with the class B amplifier design is that it can create distortion at the zero-crossing point of the waveform.

Overcome:

To overcome this zero-crossing distortion (also known as Crossover Distortion) class AB amplifiers were developed.

Outcome:

Class B Amplifier - is twice as efficient as class A amplifiers with a maximum theoretical efficiency of about 70% because the amplifying device only conducts (and uses power) for half of the input signal.

All semiconductor devices are very sensitive to temperature variations. If the temperature of a transistor exceeds the permissible limit, the transistor may be *permanently damaged. Silicon transistors can withstand temperatures upto 250°C while the germanium transistors can withstand temperatures upto 100°C.

There are two factors which determine the operating temperature of a transistor *viz.* (*i*) surrounding temperature and (*ii*) power dissipated by the transistor.

When the transistor is in operation, almost the entire heat is produced at the collector-base junction. This power dissipation causes the junction temperature to rise. This in turn increases the collector current since more electron-hole pairs are generated due to the rise in temperature. This produces an increased power dissipation in the transistor and consequently a further rise in temperature. Unless adequate cooling is provided or the transistor has built-in temperature compensation circuits to prevent excessive collector current rise, the junction temperature will continue to increase until the maximum permissible temperature is exceeded. If this situation occurs, the transistor will be permanently damaged.

The unstable condition where, owing to rise in temperature, the collector current rises and continues to increase is known as **thermal runaway.**

Thermal runaway must always be avoided. If it occurs, permanent damage is caused and the transistor must be replaced.

12.12 Heat Sink

Heat Sink

As power transistors handle large currents, they always heat up during operation. Since transistor is a temperature dependent device, the heat generated must be dissipated to the surroundings in order to keep the temperature within permissible limits. Generally, the transistor is fixed on a metal sheet (usually aluminium) so that additional heat is transferred to the *Al* sheet.

The metal sheet that serves to dissipate the additional heat from the power transistor is known as **heat sink.**

Most of the heat within the transistor is produced at the **collector junction. The heat sink increases the surface area and allows heat to escape from the collector junction easily. The result is that temperature of the transistor is sufficiently lowered. Thus heat sink is a direct practical means of combating the undesirable thermal effects *e.g.* thermal runaway.

* Almost the entire heat in a transistor is produced at the collector-base junction. If the temperature exceeds the permissible limit, this junction is destroyed and the transistor is rendered useless.

** Most of power is dissipated at the collector-base junction. This is because collector-base voltage is much greater than the base-emitter voltage, although currents through the two junctions are almost the same.

It may be noted that the ability of any heat sink to transfer heat to the surroundings depends upon its material, volume, area, shape, contact between case and sink and movement of air around the sink. Finned aluminium heat sinks yield the best heat transfer per unit cost.

It should be realised that the use of heat sink alone may not be sufficient to prevent thermal runaway under all conditions. In designing a transistor circuit, consideration should also be given to the choice of (*i*) operating point (*ii*) ambient temperatures which are likely to be encountered and (*iii*) the type of transistor *e.g.* metal case transistors are more readily cooled by conduction than plastic ones. Circuits may also be designed to compensate automatically for temperature changes and thus stabilise the operation of the transistor components.

12.13 Mathematical Analysis

The permissible power dissipation of the transistor is very important item for power transistors. The permissible power rating of a transistor is calculated from the following relation :

$$P_{total} = \frac{T_{J\,max} - T_{amb}}{\theta}$$

where P_{total} = total power dissipated within the transistor

$T_{J\,max}$ = maximum junction temperature. It is 90°C for *germanium* transistors and 150°C for *silicon* transistors.

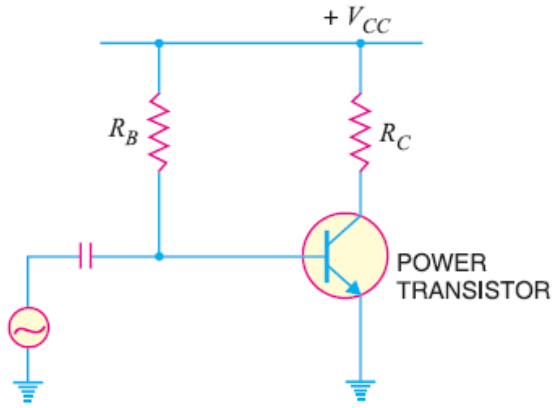
T_{amb} = ambient temperature *i.e.* temperature of surrounding air

The unit of θ is °C/ watt and its value is always given in the transistor manual. A low thermal resistance means that it is easy for heat to flow from the junction to the surrounding air. The larger the transistor case, the lower is the thermal resistance and *vice-versa*. It is then clear that by using heat sink, the value of θ can be decreased considerably, resulting in increased power dissipation.

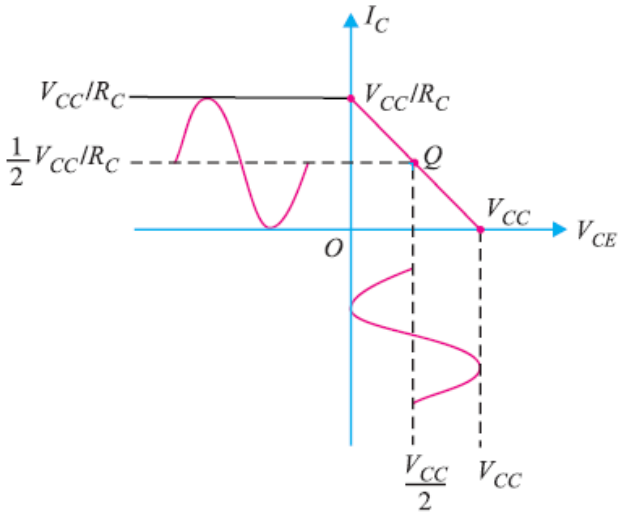
1. Explain working of series fed directly coupled Class A amplifier, also give their advantages and disadvantages.

12.8. Maximum Collector Efficiency of Series-Fed Class A Amplifier

Fig. 12.6 (*i*) shows a **series – fed class *A* amplifier. This circuit is seldom used for power amplification due to its poor collector efficiency. Nevertheless, it will help the reader to understand the class *A* operation. The d.c. load line of the circuit is shown in Fig. 12.6 (*ii*). When an *ac* signal is applied to the amplifier, the output current and voltage will vary about the operating point *Q*. In order to achieve the maximum symmetrical swing of current and voltage (to achieve maximum output power), the *Q* point should be located at the centre of the *dc* load line. In that case, operating point is $I_C = V_{CC}/2R_C$ and $V_{CE} = V_{CC}/2$.



(*i*)



(*ii*)

$$\text{Maximum } v_{ce\,(p-p)} = V_{CC}$$

$$\text{Maximum } i_{c\,(p-p)} = V_{CC}/R_C$$

$$\text{Max. } ac \text{ output power, } P_{o\,(max)} = \frac{v_{ce\,(p-p)} \times i_{c\,(p-p)}}{8} = \frac{V_{CC} \times V_{CC}/R_C}{8} = \frac{V_{CC}^2}{8R_C}$$

$$\text{D.C. power supplied, } P_{dc} = V_{CC}\, I_C = V_{CC}\left(\frac{V_{CC}}{2R_C}\right) = \frac{V_{CC}^2}{2R_C}$$

$$\therefore \quad \text{Maximum collector } \eta = \frac{P_{o(max)}}{P_{dc}} \times 100 = \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} \times 100 = 25\%$$

* $$\text{r.m.s. value} = \frac{1}{2}\left[\frac{\text{peak-to-peak value}}{\sqrt{2}}\right]$$

$$= 0.5 \times 0.707 \times \text{peak-to-peak value}$$

** Note that the input to this circuit is a large signal and that transistor used is a power transistor.

Thus the maximum collector efficiency of a class *A* series-fed amplifier is 25%. In actual practice, the collector efficiency is far less than this value.

.

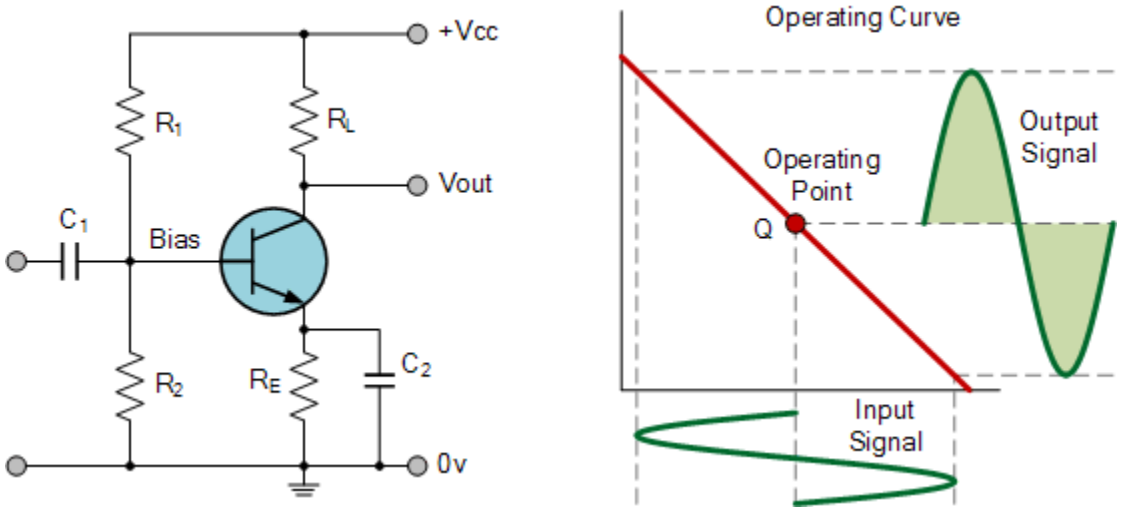
The purpose of class A bias is to make the amplifier relatively free from distortion by keeping the signal waveform out of the region between 0V and about 0.7V where the transistor's input characteristic is non linear.

Class A design produces good linear amplifiers, but are waste of power. The output power they produce is theoretically 50%, but practically only about 30 to 40%.

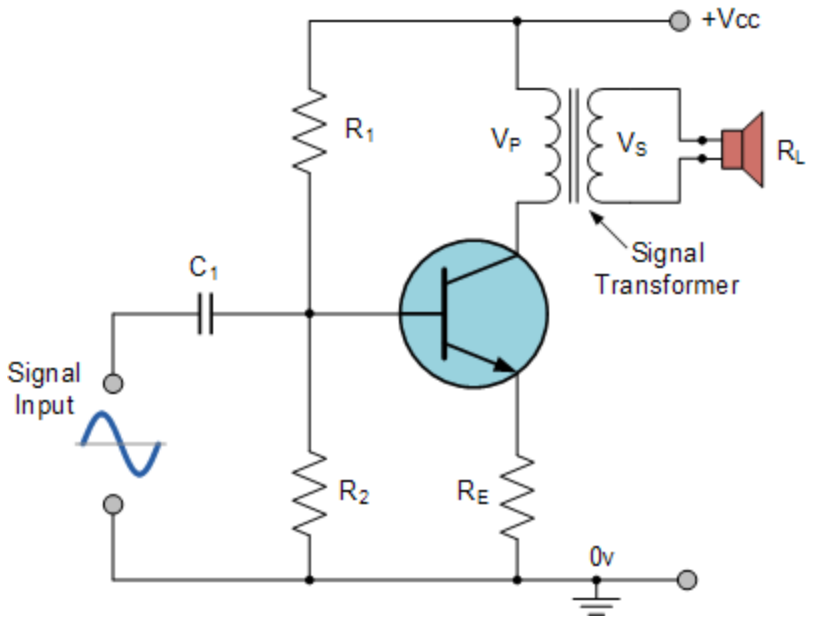
Characteristics:

To achieve high linearity and gain, the output stage of a class A amplifier is biased "ON" (conducting) all the time. As a class A amplifier operates in the linear portion of its characteristic curves, the single output device conducts through a full 360 degrees of the output waveform.

Class A Power Amplifier



Transformer – Coupled Class A Power Amplifier



With V_{CC} supply, the magnetic flux in the transformer core causes an induced emf in the transformer primary windings. This causes an instantaneous collector voltage to rise to a value of twice the supply voltage 2Vcc giving a maximum collector current of twice Ic.

Efficiency:

The ratio of the AC output power delivered to the load to DC input power applied is referred to as conversion efficiency. It is also called as collector circuit efficiency in case of transistor amplifier.

$$Efficiency\ (\eta) = \frac{power\ delivered\ to\ the\ load}{d.c.\ power\ taken\ from\ the\ supply} = \frac{Pout}{Pin}$$

The r.m.s. Collector voltage is given as:

$$V_{CE} = \frac{V_{C(max)} - V_{C(min)}}{2\sqrt{2}} = \frac{2V_{CC} - 0}{2\sqrt{2}}$$

The r.m.s. Collector current is given as:

$$I_{CE} = \frac{I_{C(max)} - I_{C(min)}}{2\sqrt{2}} = \frac{2I_{C} - 0}{2\sqrt{2}}$$

The r.m.s. Power delivered to the load (Pac) is therefore given as:

$$P_{ac} = V_{CE} \times I_{CE} = \frac{2V_{CC}}{2\sqrt{2}} \times \frac{2I_C}{2\sqrt{2}} = \frac{2V_{CC}\,2I_C}{8}$$

The average power drawn from the supply (Pdc) is given by:

$$P_{dc} = V_{CC} \times I_C$$

and therefore the efficiency of a Transformer-coupled Class A amplifier is given as:

$$\eta_{(max)} = \frac{P_{ac}}{P_{dc}} = \frac{2V_{CC}\,2I_C}{8V_{CC}I_C} \times 100\%$$

Drawbacks:

As the output device is "ON" at all times, it is constantly carrying current, which represents a continuous loss of power in the amplifier. Due to this continuous loss of power class A amplifiers create tremendous amounts of heat adding to their very low efficiency at around 30-40%, making them impractical for high-power amplifications.

Also one big disadvantage of this type of circuit is the additional cost and size of the audio transformer required.

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15.15 Tuned Class C Amplifier

So far we have confined our attention to tuned class *A* amplifiers. Such amplifiers are used where *RF* signal has low power level *e.g.* in radio receivers, small signal applications in transmitters. However, owing to low efficiency of class *A* operation, these amplifiers are not employed where large *RF* (radio frequency) power is involved *e.g.* to excite transmitting antenna. In such situations, tuned class *C* power amplifiers are used. Since a class *C* amplifier has a very high efficiency, it can deliver more load power than a class *A* amplifier.

Class *C* operation means that collector current flows for less than 180°. In a practical tuned class *C* amplifier, the collector current flows for much less than 180° ; the current looks like narrow pulses as shown in Fig. 15.17. As we shall see later, when narrow current pulses like these drive a high-*Q* resonant (*i.e. LC*) circuit, the voltage across the circuit is almost a perfect sine wave. One very important advantage of class *C* operation is its *high efficiency. Thus 10 W supplied to a class *A* amplifier may produce only about 3.5 W of a.c. output (35 % efficiency). The same transistor biased to class *C* may be able to produce 7 W output (70 % efficiency). Class *C* power amplifiers normally use *RF* power transistors. The power ratings of such transistors range from 1 W to over 100 W.

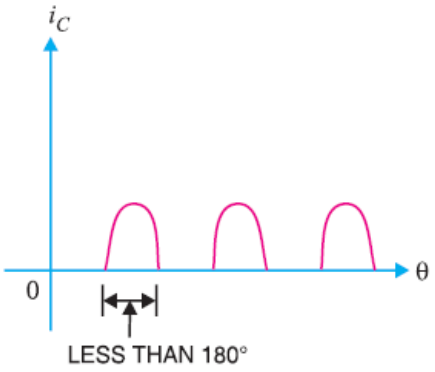


Fig. 15.17

15.16 Class C Operation

Fig. 15.18 (*i*) shows the circuit of tuned class *C* amplifier. The circuit action is as under:

(*i*) When no a.c. input signal is applied, no collector current flows because the emitter diode (*i.e.* base-emitter junction) is unbiased.

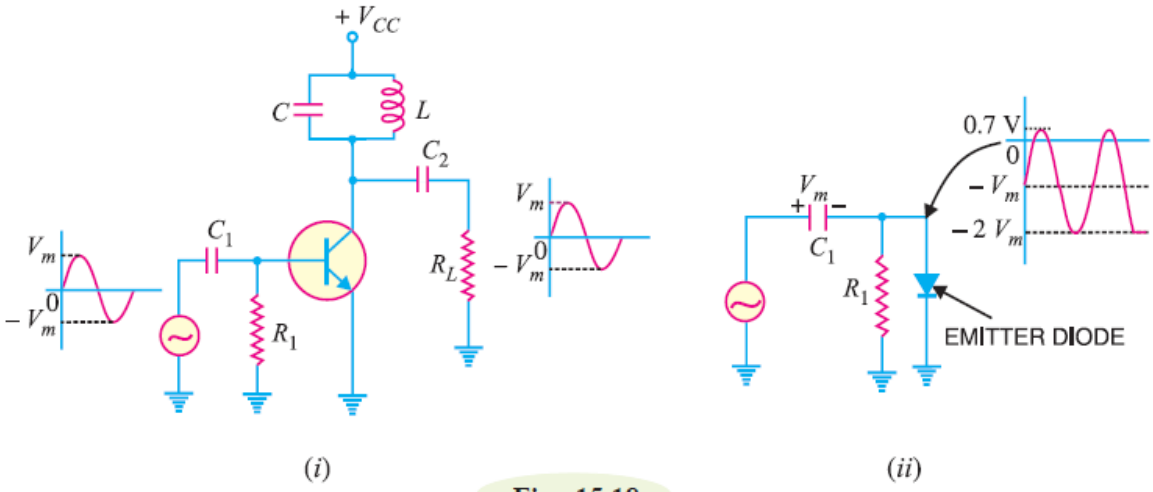


Fig. 15.18

(*ii*) When an a.c. signal is applied, *clamping action* takes place as shown in Fig. 15.18 (*ii*). The voltage across the emitter diode varies between + 0.7 V (during positive peaks of input signal) to about $-2V_m$ (during negative peaks of input signal). This means that conduction of the transistor occurs only for a short period during positive peaks of the signal. This results in the pulsed output *i.e.* collector current waveform is a train of narrow pulses (Refer back to Fig. 15.17).

(*iii*) When this pulsed output is fed to the *LC* circuit, **sine-wave output is obtained. This can be easily explained. Since the pulse is narrow, inductor looks like high impedance and the capacitor like a low impedance. Consequently, most of the current charges the capacitor as shown in Fig. 15.19.

UNIT - IV

32.11. Monostable Multivibrator

It is also called *one shot* or *univibrator* and can be used to generate a gating pulse, whose width can be controlled. The monostable moltivibrator provides a single pulse of desired duration in response to an *external trigger. The external trigger causes the circuit to go to the quasi-stable state. After a certain interval of time, the circuit returns to its original stable state.

Figure 32.4 shows the circuit of a monostable multivibrator using NPN transistors. Here, the output of transistor Q_2 is coupled to the base of transistor Q_1 through the resistance R_1. On the other hand, the output of transistor Q_1 is coupled to the base of transistor Q_2 through the capacitor C_2. The capacitor C_1 is known as commutating capacitor or speed up capacitor. Its function is to speed up the circuit in making abrupt transitions between the ON and OFF states. The base of transistor Q_2 is returned to the V_{CC} supply through a resistor R_3, while the base of transistor Q_1 is connected to the negative supply through a resistor R_2. The advantage of this biasing is that it keeps the transistor Q_1 OFF and Q_2 ON. This state is known as a stable state of the monostable multivibrator.

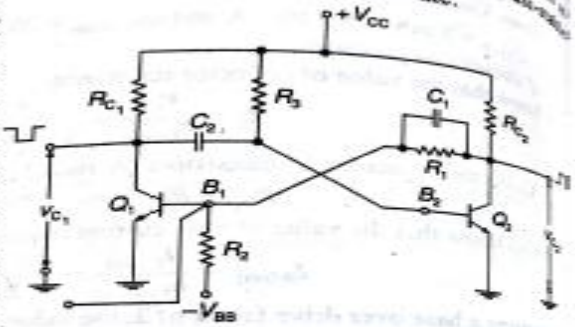


Fig. 32.7. Monostable multivibrator.

The output of a monostable multivibrator is available at the collector terminal of either

The circuit operation may be explained by keeping in mind that initially the circuit is in its stable state i.e., Q_1 is OFF and Q_2 is ON. Now Let us see as to what happens when the trigger is applied:

1. When a positive trigger pulse of sufficient amplitude is applied to the base of transistor Q_2, it overrides the reverse bias provided by the V_{BB} supply and gives it a forward bias. Because of this, the transistor Q_2 starts conducting.
2. As the transistor Q_2 conducts, its collector voltage falls due to the voltage drop across resistor R_{C_2}. This fall in voltage is coupled through capacitor C_2, which decreases the forward bias of transistor Q_1.
3. Because of the reduced forward bias, the collector current of transistor Q_1 starts decreasing and its collector voltage rises exponentially towards $V_{CC} \cdot R_3/(R_3 + R_{C_1})$ with a time constant $\tau_2 = C_1 \cdot (R_3 \| R_{C_1})$.
4. The rising collector voltage of transistor Q_1 is coupled to the base of transistor Q_2 through resistor R_2, where it further increases its forward bias. Because of the increased forward bias, the transistor Q_2 conducts more. This action is cummulative because of the positive feedback, and the collector voltage of harrisor Q_2 falls to $V_{CE(sat)}$.
5. Immediately, the capacitor C_2 starts charging exponentially towards V_{CC} with a time constant $\tau_1 = R_3 \cdot C_2$. As C_2 charges, the voltage at the base of the transistor Q_2 decreases. As C_2 charges further, the transiator Q_2 is pulled out from the cut-off and the reverse transition takes place i.e., Q_2 turns ON and Q_1 turns OFF.
6. When the transistor Q_2 starts conducting, its collector voltage falls because of the drop across resistor R_{C_2}. This drop is coupled to the base of the transiator Q_1, whose collector voltage rises towards V_{CC} with time constant $\tau_3 = R_{C_1} \cdot C_1$. Finally, the transistor Q_1 turns fully ON and the transistor Q_2 goes OFF. The circuit remains in this stable state till another pulse is applied.

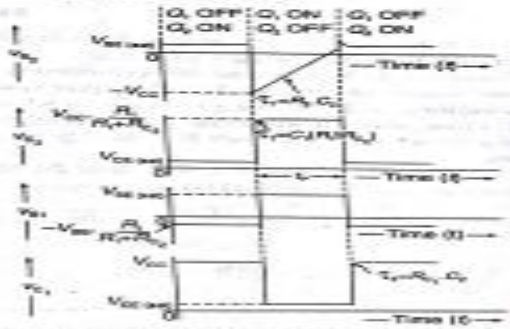


Fig. 32.8. Waveforms at the base and collector of transistor Q_1 and Q_2 of a monostable multivibrator.

Figure 32.8 shows the waveforms at the base and collector of the transistor Q_1 and Q_2 of a monostable multivibrator. The width or duration of the pulse obtained at the collector or output of either transistor (Q_1 or Q_2) of the monostable multivibrator is given by the expression,

$$t_p = 0.69 \; R_3 \cdot C_1$$

32.14. Schmitt Trigger

Figure 32.13 shows the circuit of a Schmitt trigger (after the name of its inventor). It may be noted that the circuit, is, somewhat, like multivibrator circuits. The Schmitt trigger is used for *waveshaping circuits*. It can be used for generation of square wave from a sine-wave input. Basically, the circuit has two opposite operating states as in all other multivibrator circuits. However, the trigger signal is not, typically, a pulse waveform but a slowly varying a.c. voltage. The Schmitt trigger is level sensitive and switches the output state at two distinct trigger levels. One of the triggering levels is called a *lower-trigger level* (abbreviated as L.T.L) and the other as *upper-trigger level* (abbreviated as U.T.L.).

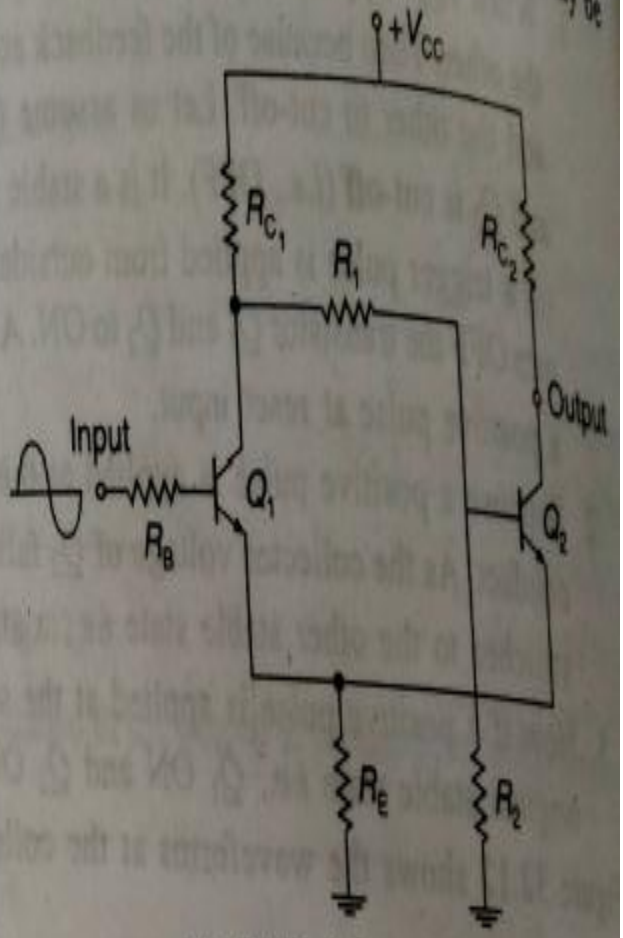


Fig. 32.13. Schmitt Trigger.

The circuit of a Schmitt trigger consist of two identical transistors Q_1 and Q_2 coupled through an emitter R_E. The resistors R_1 and R_2 form a voltage divider across the V_{CC} supply and ground. These resistors provide a small forward bias on the base of transistor Q_2. The operation of the circuit may be explained as follows:

Let us suppose that initially there is no signal at the input. Then as soon as the power supply V_{CC} is switched on, the transistor Q_2 starts conducting. The flow of its current through resistor R_E produces a voltage drop across it. This voltage drop acts as a reverse bias across the emitter-base junction of transistor Q_1 due to which it cuts-off. As a result of this, the voltage at its collector rises to V_{CC}. This rising voltage is coupled to the base of transistor Q_2 through the resistor R_1. It increases the forward bias at the base of transistore Q_2 and therefore drives it into saturation and holds it there. At this instant, the collector voltage, levels are $v_{C_1} = V_{CC}$ and $v_{C_2} = v_{CE\,(sat)}$ as shown in Figure 32.14.

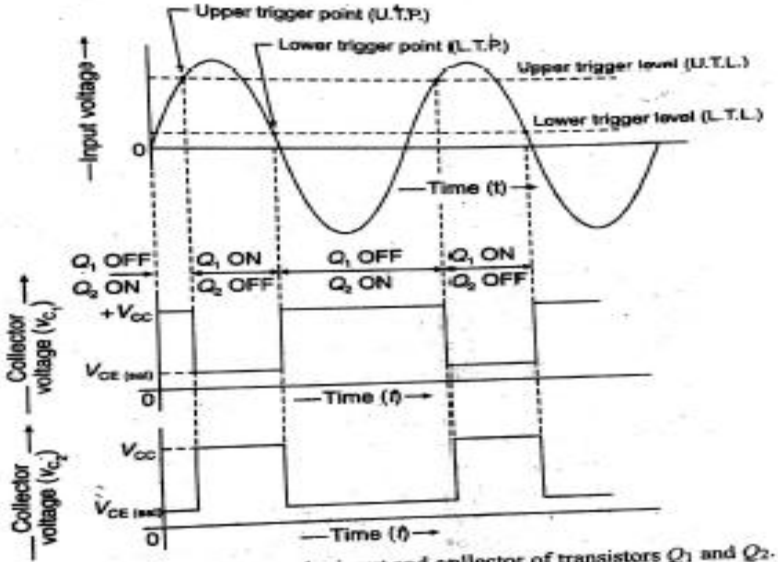


Fig. 32.14. Waveforms at the input and collector of transistors Q_1 and Q_2.

Now suppose an a.c. signal is applied at the input of the Schmitt trigger (*i.e.*, at the base of the transistor Q_1). As the input voltage increases above zero, nothing will happen until it crosses the upper trigger level (U.L.T.). As the input voltage increases, above the upper-trigger level, the transistor Q_1 conducts. *The point, at which it starts conducting, is known as upper-trigger point* (U.T.P.). As the transistor Q_1 conducts, its collector voltage falls below V_{CC}. This fall is coupled through resistor R_1 to the base of transistor Q_2 which reduces its forward bias. This in turn reduces the current of transistors Q_2 and hence the voltage drop across the resistor R_E. As a result of this, the reverse bias of transistor Q_1 is reduced, and it conducts more. As the transistor Q_1 conducts more heavily, its collector current further reduces due to which the transistor Q_2 conducts near cut-off. This process continues till the transistor Q_1 is driven into saturation and Q_2 At this instant, the collector voltage levels are $V_{C_1} = V_{CE\,(sat)}$ and $V_{C_2} = V_{CC}$ as shown i

The transistor Q_1 continue to conduct *till the input voltage falls below the lower-* (L.T.L.). It will be interesting to know that when the input voltage becomes lower-trigger level, the emitter-base junction of transistor Q_1 becomes reverse biase of this, its collector voltages starts rising towards V_{CC}. This rising voltage increase bias across transistor Q_2, due to which it conducts. *The points, at which transis conducting is called lower-trigger point* (L.T.P.). Soon the transistor Q_2 is driven i and Q_1 to cut-off. This completes one cycle. The collector voltage levels at this ins V_{CC} and $V_{C_2} = V_{CE\,(sat)}$. No change in state will occur during the negative half cycl voltage.

It is evident from the above discussion that the output of a Schmitt trigger is a pulse, whose width depends upon the time during which transistor Q_1 is co onduction time is set by the upper- and lower-trigger levels.

Clipper is a circuit with which the waveform is shaped by removing (or clipping) a portion of the applied waveform above or below a certain level.

Clipper finds wide use in radar communicaiton, digital and other electronic systems. Even though several clippers have been developed to change the waveshape, we shall focus our attention to diode clippers. The clippers may be classified as Positive clipper, Negative clipper, Biased clipper and Combination clipper.

1. Positive Clipper : A positive Clipper is one which removes the positive half–cycles of the applied input voltage.

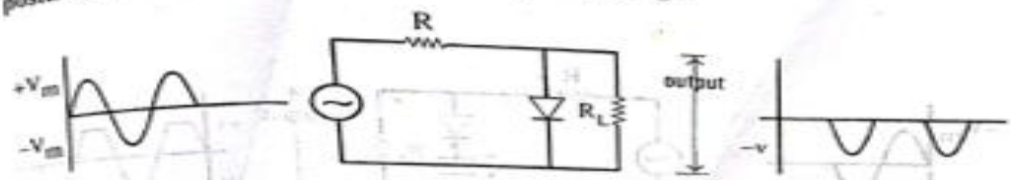


Fig 1.28 Positive clipper

Figure shows the circuit of a positive clipper using a diode. As indicated, the output voltage has all the positive half– cycles removed or clipped. The circuit working is as follows: During the positive half cycle of the input voltage, the diode is forward biased and it is conducting heavily. Therefore the voltage across the diode is zero(considering it as ideal diode) hence across the load R_L, the voltage is zero. Therefore the output voltage during positive half cycles become zero.

During the negative half cycle of the input voltage, the diode is at reverse bias condition hence behaves as an open circuit. At this condition, the circuit acts as a voltage divider.

The output voltage will be $\frac{R_L}{R + R_L} Vm$

Generally $R_L >> R$

therefore, output voltage = –Vm.

2. Negative Clipper : If it is decided to remove the negative half cycle of the input. the only thing to be done is to reverse the polarities of the PN diode in the previous circuit. The clipper is then called as **Negative Clipper.** For Negative clipper the output voltage during negative half cycle is zero. Therefore the negative half cycles are removed or clipped off.

3. Biased Clipper : If It is required to remove some portion of positive or negative half cycles of the applied signal clipper may be used. The biased clipper consists of a diode with a battery of V Volts. A portion of each positive half cycle will be clipped as shown in the diagram. However, the negative half cycles will appear without any change. This clipper is called **biasd positive clipper.**

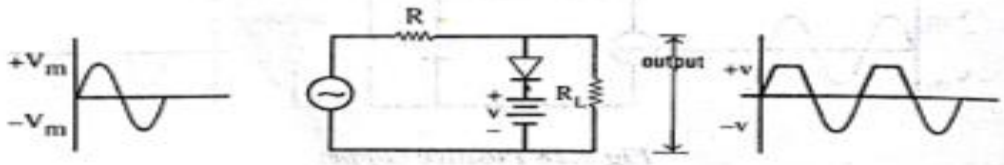


Fig 1.29 Biased Clipper

The circuit working is as following. The diode will conduct heavily so long as input voltage is larger than +V. When the input voltage is larger than +V, the diode acts as a short and the output is equal to +V. The output will be +V so long as the input voltage is higher than +V. During the period the input voltage is lesser than +V, the diode is at reverse bias and behaves as an open circuit. Therefore, most of the applied input voltage appears across the output. This is the process being adopted by the biased positive clipper to remove input voltage above +V. During the negative half cycle of the input voltage, the diode remains at reverse bias hence the negative half cycles appear across the load. If it is required to remove a portion of negative half cycles of input voltage, the only thing to be followed is to reverse the polarities of the battery or the diode. Then the circuit will be called as **biased negative clipper.**

4. Combination Clipper : Combination clipper is a combination of biased positive and negative clippers. With a combination clipper, a portion of both positive and negative half cycles of input voltage can be clipped or removed.

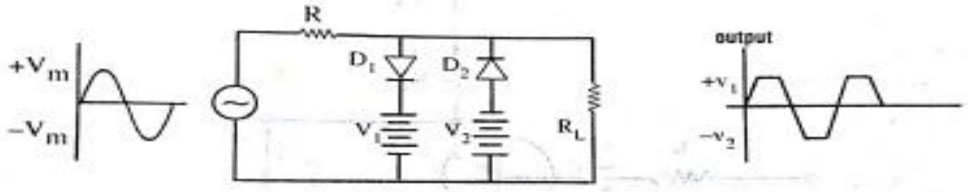


Fig 1.30 Combination Clipper

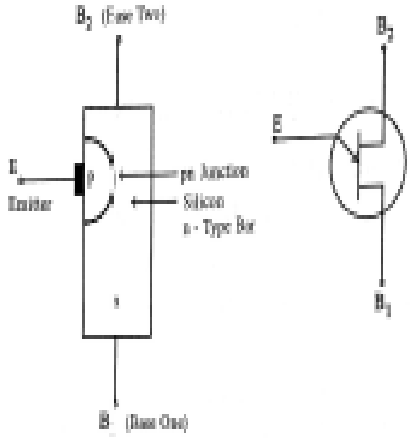
The circuit working is as follows. When positive input voltage is larger than $+V_1$, the diode D_1 is conducting heavily while diode D_2 is at reverse bias. Therefore, the voltage $+V_1$, drops across the load. The output remains at $+V_1$ as long as the input voltage exceeds $+V_1$. During the negative half cycle, the diode D_2 is conducting heavily and the output remains at $-V_2$ as long as the input voltage is larger than –V2. Between $+V_1$ and $-V_2$ no diode is on. At this condition, the applied input voltage appears at the load.

Applications of Clipper :

1. Clipper circuits are oftenly used in radar applications.
2. Clippers are used in digital computers.
3. Clippers finds wide use in radio and Television receivers

Construction

UJT consists of an n-type Silicon bar with two leads at the end. The leads are called base-one B_1 and base -two B_2. A Pn junction is formed between a P-type emitter and the bar. The lead to this junction is known as emitter E. The emitter is nearer to B_2 than B_1. Fig shows symbol for UJT.



(a) Fig 3.17 (b)

The collector has only one Pn junction and therefore called as unijunction transistor. Having only one Pn junction device is looking like a diode. Because the two base terminals are taken from the Silicon bar hence it is called as **double based diode.** The emitter is heavily doped. The n region is lightly doped. Therefore the resistance between the base terminals is very high (5 to 10 KΩ) when emitter lead is kept open.

Working :

1. The device has normally B_2 positive withrespect to B_1. If voltage is V_{BB} is given between B_2 and B_1 with emitter open, a voltage gradient is formed along the n-type bar. The emitter is located nearer to B_2. Therefore more than half of V_{BB} drops between the emitter and B_1.

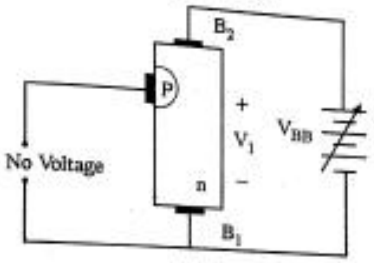
2. The voltage V_1 between emitter and B_1 makes a reverse bias Pn junction the emitter current is stopped. Due to reverse bias a small leakage current flows from B_2 to emitter due to minoritiy carriers.

3. If a positive voltage is given at the emitter terminal, the Pn junction will continue reverse bias as long as the input voltage is less than V_1.

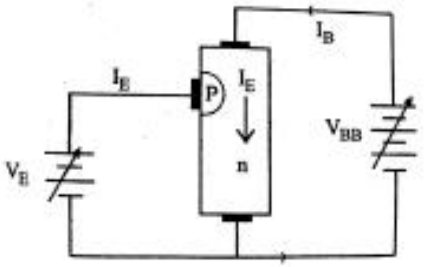
4. Let the input voltage to the emitter exceeds V_1, then Pn junction becomes forward biased. Now, holes are injected from P type material into the n type Silicon bar.

5. The B_2 terminal is repelling these holes while B_1 terminal attracts them. This formation of holes in the emitter to B_1 region results in the decrease of resistance in this portion of the bar.

6. As a result the internal drop from emitter to B_1 is increased. Therefore the emitter current I_E increases.



(a) Fig 3.18



(b) Fig 3.18

7. As more holes are introduced a condition of saturation will g reached. Now the emitter current is controlled by emitter power suppl only. The device is now at **ON** state.

8. If a negative pulse is given to the emitter then the Pn junction i reverse biased and the emitter current is cut off. Now, the UJT is at **OFF** State.

Equivalent Circuit :

The equivalent circuit is shown in the figure. The resistance offered by the Silicon bar is called inter-base resistance R_{BB}. The inter base resistance is denoted by two resistors in series.

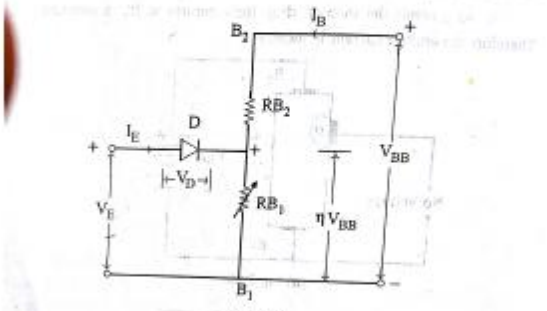


Fig 3.19

R_{B2} is the resistance between B_2 and the point at which the emitter junction lies. R_{B1} is the resistance available between B_1 and emitter junction. R_{B1} is shown as variable. The reason is depending upon the bias voltage across the Pn junction. The Pn junction is formed in the emitter by a diode D. If no voltage is applied to the UJT, the inter base resistance becomes

$$R_{BB} = R_{B1} + R_{B2}$$

The value of R_{BB} generally lies between 4KΩ and 10 KΩ. If a voltage V_{BB} is introduced between the base terminals keeping the emitter open, the voltage will be divided across R_{B1} and R_{B2}. Voltage across R_{B1} is

$$V_1 = \frac{R_{B_1}}{R_{B1} + R_{B2}} V_{BB}$$

$$V_1 / V_{BB} = R_{B1} / R_{B1} + R_{B2}$$

The ratio V1 / V_{BB} is known as **instrinsic stand off ratio .** It is denoted by Greek letter η.

$$\eta = \frac{R_{B_1}}{R_{B1} + R_{B2}}$$

The value of η usually available between 0.51 and 0.82

$$VR_{B1} = \eta V_{BB}$$

The voltage ηV_{BB} dropping across R_{B1} reverse biases the diode. As a result the emitter current becomes zero. If a rising positive voltage is applied to the emitter, the diode will become forward biased. When the input voltage exceeds ηV_{BB} by V_D, the forward bias voltage drop across the Silicon diode.

$$V_P = \eta V_{BB} + V_D$$

Where

V_P – Peak point voltage

V_D – forward voltage drop across Silicon diode (0.7V).

When the diode D is conducting, holes are injected from P-type material to the n-type bar. These holes are swept down towards the B_1 terminal. This decreases the resistance between emitter and B_1. Therefore

EMITTER CHARACTERISTICS OF UJT

The graph shows the curve between emitter voltage (V_E) and the emitter current (I_E) of UJT.

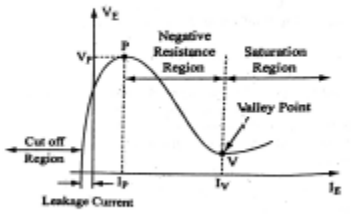


Fig 3.20

1. In the cut-off Region, as the emitter voltage increases a small leakage current passes through the device.
2. After reaching certain emitter voltage V_E , The emitter voltage reaches the peak point P.At this point, peak voltage Vp and peak current Ip. If Ie current is still increased the emitter voltage Ve starts decreasing. This region is called as Negative Resistance Region.
3. The Negative Resistance Region is continuing until valley point V is reached. After the valley point , the UJT is drain to saturation.

UJT Relaxation Oscillator

The UJT relaxation oscillator is as shown in the figure. The discharging of a capacitor through UJT can develop a saw tooth output.

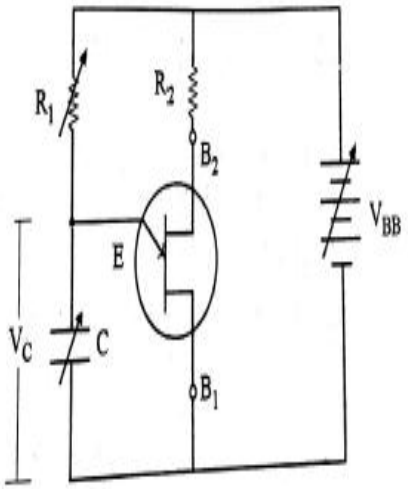
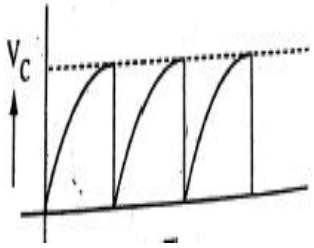


Fig 3.21 (a)



When the battery V_{BB} is on, the capacitor C starts charging through resistor R_1. During the charging period the voltage across the capacitor increases in an exponential relation upto reaching the peak point voltage. At this instant UJT switches to its low resistance conducting mode and the capacitor is starts discharging between E and B_1. As the capacitor voltage moves back to zero, the UJT is switched off. The next cycle is beginning by allowing the capacitor C to charge again. The output sawtooth waveform frequency can be varied by changing the value of R_1. Because the resistor R_1 controls the time constant R_1C of the capacitor charging circuit. The voltage V_c across the capacitor prior to breakdown is

$$V_c = V_{BB}\left(1 - e^{-t/r_1 c}\right)$$

The time period is

$$t = 2.3\, R_1\, C \log_{10} \frac{1}{1-\eta}$$

The frequency of sawtooth wave is

$$f = \frac{1}{t\ (\text{in seconds})}\ \text{Hz.}$$

8. Astable Multivibrator

t is also called a *free-running relaxation oscillator* and is commonly used to generate square eform. Figure 32.4 shown the circuit of a collector-coupled astable multivibrator using two tical NPN transistors Q_1 and Q_2. It is possible to have $R_{C_1} = R_{C_2} = R_C$, $R_1 = R_2 = R$ and $C_1 = C$. In that case, the circuit is known as symmetrical astable multivibrator. The transistor Q_1 orward biased by the V_{CC} supply ugh resistor R_1. Similarly, the sistor Q_2 is forward biased by the supply through resistor R_2. The put of transistor Q_1 is coupled to input of transistor Q_2 through the acitor C_1. Similarly, the output of nsistor Q_2 is coupled to the input of sistor Q_1 through the capacitor C_2.

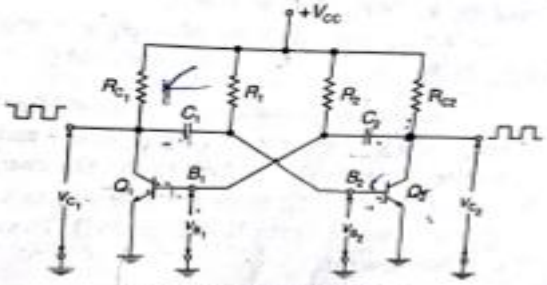


Fig. 32.4. Astable multivibrator.

32.9. Circuit Operation of Astable Multivibrator

The circuit operation of an astable multivibrator is easy to understand with the waveforms shown in Figure 32.5. These waveforms are at the base and collector of transistors Q_1 and Q_2. Figure 32.5 (*a*) shows the waveform for the base voltage of transistor Q_1 (*i.e.*, v_{B_1}) and Figure 32.5 (*b*) for the collector voltage of transistor Q_1 (*i.e.*, v_{C_1}). Similarly Figure 32.5 (*c*) shows the waveform for the base voltage of transistor Q_2 (*i.e.*, v_{B_2}) and Figure 32.5 (*d*) for the collector voltage of transistor Q_2 (*i.e.*, v_{C_2}). The circuit operation may be explained as follows:

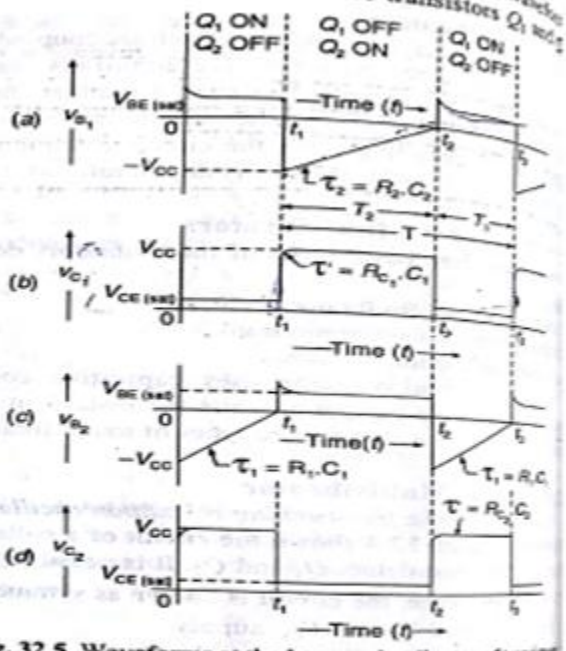


Fig. 32.5. Waveforms at the base and collector of transistors Q_1 and Q_2 in astable multivibrator.

1. When the d.c. power supply (V_{CC}) is switched ON, (say at $t = 0$) one of the transistor will start conducting more than the other due to some imbalance in the circuit. Let us suppose that transistor Q_1 start conducting more than that of transistor Q_2. Then because of positive feedback, the transistor Q_1 will be driven into saturation and transistor Q_2 to cut-off. Thus at $t > 0$, the transistor Q_1 is ON and Q_2 is OFF. Thus at $t > 0$, $v_{B_1} = V_{BE\,(sat)}$ (*i.e.*, 0.7 V for silicon transistor), $V_{C_1} = V_{CE\,(sat)}$ (*i.e.*, 0.3 V for silicon transistor), v_{B_2} is negative and $V_{C_2} = V_{CC}$.
2. During the time $t > 0$ (*i.e.*, when Q_1 is ON and Q_2 is OFF), the capacitor C_1 is charging towards the voltage V_{CC} through R_1. The charging takes place exponentially with time constant $\tau_1 = R_1 \cdot C_1$. Since the base of transistor Q_2 is directly connected to capacitor C_1, as shown in Figure 32.4 (page 597). Therefore the voltage V_{B_2} also increases exponentially towards V_{CC}.

3. As soon as the voltage V_{B_2} increases, above the cut-in voltage (*i.e.*, 0.5 V for silicon transistor), the transistor Q_2 starts conducting. It occurs at t = t_1. As the transistor Q_2 goes into saturation, its collector voltage (v_{C_2}) falls to $v_{CE(sat)}$. The fall in voltage v_{C_2} causes an equal fall, (*i.e.*, $V_{CC} - V_{CE_{(sat)}} = V_{CC}$) in voltage v_{B_1} because the two are capacitively coupled. The fall in voltage v_{B_1} cuts-off the transistor Q_1 and its collector voltage (v_{C_1}) starts rising towards V_{CC} with a time constant $\tau' = R_C \cdot C_1$. The rise in voltage V_{C_1} is coupled through capacitor C_1 to the base of the transistor Q_2, causing a small overshoot in voltage v_{B_2}. Soon the voltage V_{B_2} settles at $V_{BE(sat)}$ *i.e.*, 0.7 V level. Thus at $t \geq t_1$, the transistor Q_1 is OFF and Q_2 is ON. The voltage levels at this instant are v_{B_1} is negative, $v_{C_1} = V_{CC}$, $v_{B_2} = V_{BE} = V_{BE(sat)}$ and $v_{C_2} = V_{CE(sat)}$.

4. During the time $t > t_1$ (*i.e.*, when Q_1 is OFF and Q_2 is ON) the voltage v_{B_1} rises exponentially with time constant $\tau_2 = R_2 \cdot C_2$ towards V_{CC}. At $t = T_2$, the voltage v_{B_1} reaches the cut-in level (*i.e.*, 0.5 V) and a reverse transition takes place (*i.e.*, Q_1 turns ON and Q_2 turns OFF). The voltage levels for $t > t_2$ are $v_{B_1} = v_{BE(sat)}$, $v_{C_1} = v_{CE(sat)}$; v_{B_2} is negative and $v_{C_2} = V_{CC}$. Thus the voltage levels for $t > t_2$ are the same as for $t > 0$.

may be noted that for an astable multivibrator, using PNP transistors, the voltages and nts are negative to those for a circuit with NPN transistors. Thus all the waveform shown in re 32.5 must be inverted, if PNP transistors are used.

UNIT – V

Switching voltage regulator is also known as switched mode power supply (SMPs). The working of SMPs is differing from the conventional series regulator in the following way. In series regulator, a pass transistor is used to obtain a controlled voltage drop. Whereas, in SMPs, the pass transistor can be used as a **"Controlled Switch"**. It can be operated at either saturated or cutoff state. Therefore **the power given across the pass device is in discrete pulses instead of steady current flow.** Higher efficiency is obtained since the pass device is used as a low impedance switch. If the pass device is at cutoff condition, there will be no current hence dissipates no power. When the pass device is in saturation state, a very small voltage drop occcurs across it hence dissipates only a small amount of average power, giving maximum current to the load. In both the cases, the power wasted in the transistor is very small and most of the power is transmitted to the load. Hence SMPs exhibits very goad efficiency in the range of 70–90%.

Switching regulators are available in various configurations such as flyback, push–pull, feed–forward, and nonisolated single ended or single polarity types. The switching regulators can be operated in three different modes namely; step–down, step–up or polarity inverting.

A basic switching regulator essentially consists of four parts namely;

1. Voltage sourse (Vin)
2. Switch (S)
3. Pulse generator
4. Filter (F)

The basic switching regulator is as shown in the figure.

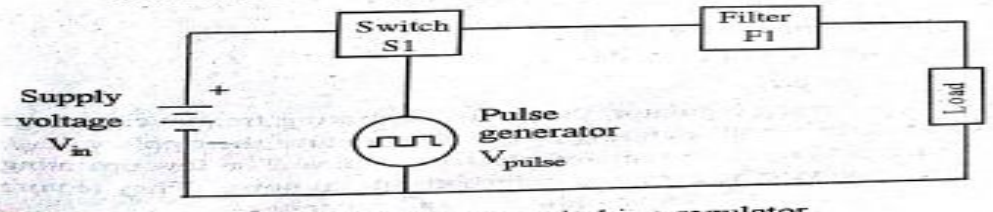


Fig. 5.34 Basic switching regulator.

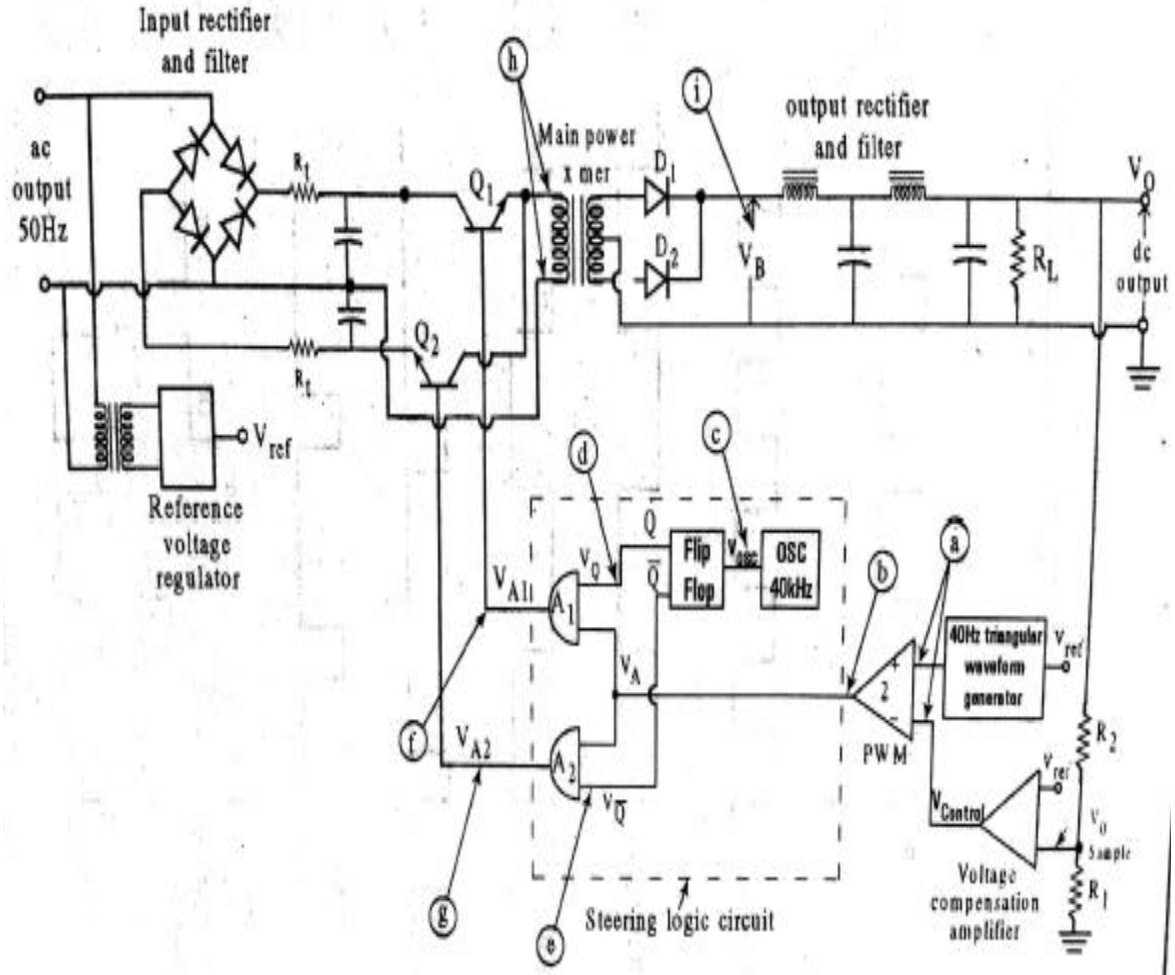


Fig 5.36 A switched mode power supply

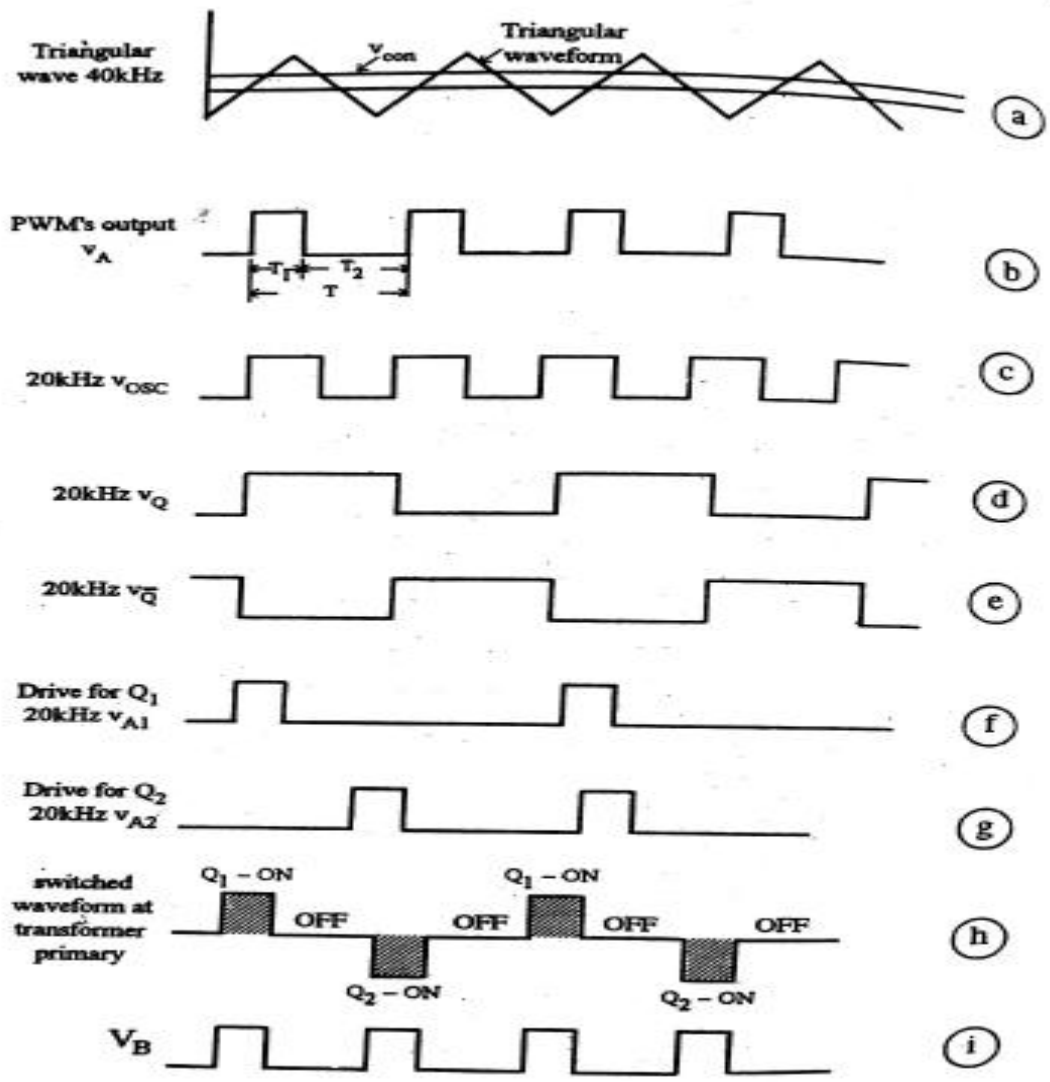


Fig 5.37 Switching power supply wave forms

The Comparator a operates as a pulse width modulator. Its output is a square wave V_A of period T. The duty cycle of the square wave is given by $\frac{T_1}{T_1+T_2}$. It Varies with V_{con} and in turn varies with the variation of V_o. The output V_A opertes a steering logic circuit shown by the dashed block. It consists of a 40kHz oscillator cascaded with O flip–flop. It produces two complementary outputs V_Q and $V_{\overline{Q}}$.

The output V_{A1} and V_{A2} of AND gates A_1 and A_2 are as shown in the figures. These waveforms are given at the base of Q_1 and Q_2. Depending upon, ON condition of Q_1 or Q_2, the waveform at the input of the transformer will be a square wave. The rectified output V_B is shown in the figure. The switched Mode power supply circuit shows that the output current flows through the power switch. The power switch consists of transistors Q_1 and Q_2, low resistance inductor and the load. By using a low loss switch and a filter with high guality factor, the conversion efficiency of 90% and more can be achieved.

Suppose, these is a rise in dc output voltage. Then V_{con} of comparator 1 rises. This changes the inter section between triangular waveform and V_{con}. As a result time period T_1 decreases. In turn, it decreses the pulse width of the waveform. Smaler the pulse width, lowers the average value of the dc output V_o. In this way, the initial rise in dc output has been nullified.

The switched Mode power supply has better performance thanlinear regulated power supply. For SMPs, very high frequency signals in the range of above 40kHz are applied. The transistors Q_1 and Q_2 are used as switches. They become alternately on and off at 20kHz. Once again Q_1 or Q_2 becomes on for a small duration and consumes negligible power. It may be observed that the high operting frequency allows the use of smaller transformers, capacitors and inductors hence decrease in size and cost are achieved.

Limitations:

1. The rectifier is connected directly to a.c line hence the rectifiers, capacitors and switching transistors must with stand the peak line voltage.
2. SMPs is more complex and needs external components like inductors and transformers.
3. SMPs is slow in responding to transient load changes compared to the conventional series regulator.
4. The Electro–magnetic and radio–frequency interference are there in SMPs.

Half-Wave Controlled Rectifier

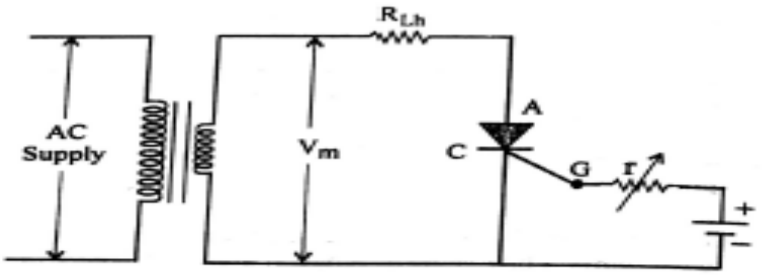


Figure 30 Halfwave controlled rectifier

In this case ac voltage connected to the SCR through the load resistance is connected in series with anode. To control the gate current, a variable resistor 'r' is inserted in the gate circuit. The ac supply to be converted into dc supply is applied to the primary of the transformer. The peak inverse voltage appearing across the secondary should be less than the reverse breakdown voltage of SCR. So that it will not breakdown during the negative half of ac supply. Otherwise a diode needs to be connected in series with a resistor 'r' to block the reverse voltage on the gate during the negative half cycle.

Operation

1. When adjusting the variable resistance r, a suitable gate current is made to flow then, SCR conducts during the positive half cycle. Suppose the gate current is adjusted to such a value that SCR closes at a positive value V_1 which is less than peak voltage V_m. So, when the secondary voltage becomes V_1 in the positive half cycles then SCR starts conducting. Beyond this voltage SCR continues to conduct till the voltage becomes zero.

2. During the negative half cycle of ac voltage, the SCR will not conduct regardless of the gate voltage because the anode is negative with respect to cathode.

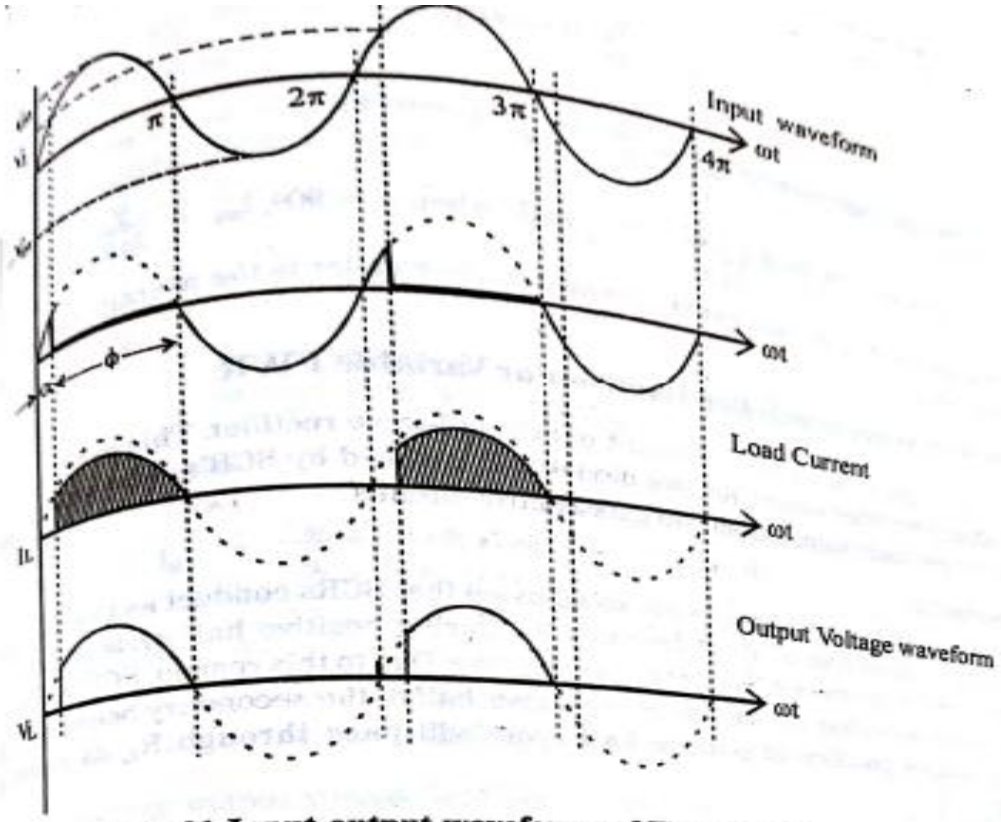


Figure 31 Input-output waveforms of HW controlled rectifier

Again at the start of the next positive half cycle, when the secondary voltage ecomes V_1, the SCR conducts. From figure 31 it is clear that firing angle is α hile the conduction angle ϕ is $(180-\alpha)$

$$\text{The average current } I_{av} = \frac{V_{av}}{R_L} = \frac{V_m}{2\pi R_L}[1+\cos\alpha] \qquad (106)$$

when $\alpha = 0^o$, then $I_{av} = \frac{V_m}{\pi R_L}$ and when $\alpha = 90^o$, $I_{av} = \frac{V_m}{2\pi R_L}$

This shows that greater the firing angle α, the smaller is the average current and viceversa

Full-Wave Controlled Rectifier

The figure 32 shows the circuit of SCR full-wave rectifier. This exactly like an ordinary rectifier except the two diodes are replaced by SCR's. The gates of both SCR's get their supply from two gate control circuits.

Operation

Suppose the gate currents are so adjusted that SCRs conduct as the secondary voltage (across half winding) becomes V_1. During positive half cycle of input the upper end is positive while lower end is negative. Due to this reason, SCR I conducts, of course only when the voltage across upper half of the secondary becomes V_1. So the shaded position of positive half cycle will pass through R_L as shown in figure 33.

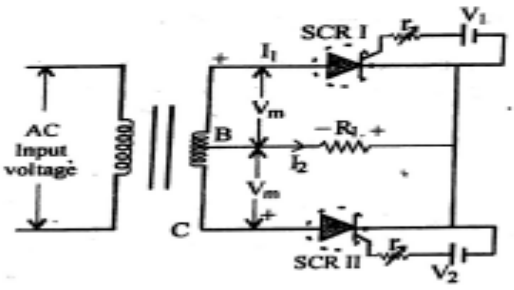


Figure 32 for controlled rectifier

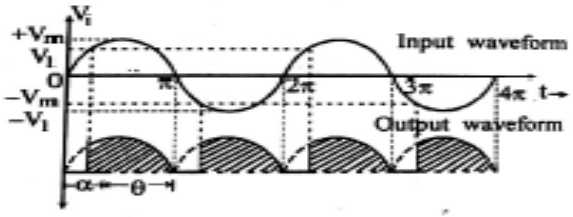


Figure 33 Output Waveform of FW controlled recitifier

During negative half cycle of ac, the upper end of secondary becomes negative while lower end becomes positive. Under this situation, SCR II conducts, only when the voltage across the lower half of the secondary becomes V_1, now a current flows

UJT Triggered Controlled Rectifier

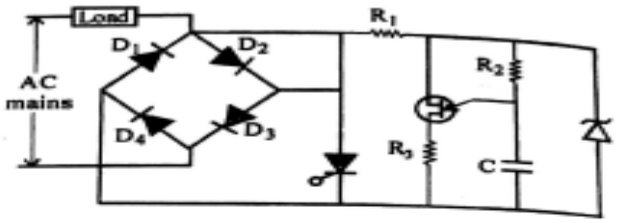


Figure 35 UJT triggered SCR phase control

UJT triggered SCR phase control

The SCR's are generally used in power control circuits. In these circuits, the conduction period of SCR can be varied by varying the voltage applied to control circuit. The value of phase angle or conduction angle controls the power delivered to the load. To deliver the maximum power the firing angle α must be zero therefore the SCR conduct for 0° to 180°. If the power requirements is below the maximum value, the firing angle lies between 0° to 180°. In order to adjust the firing angle of SCR, a control circuit is required. Such a circuit is shown in figure 35.

The operation can be explained as follows, the SCR is in OFF state until UJT fires, when the UJT fires the capacitor will discharge quickly through the resistor R_3. This positive pulse will turn ON the SCR. The SCR will remains ON, until the SCR line voltage approaches zero. At this point, the SCR will turn OFF throughout the entire negative cycle.

The output of a rectifier circuit consists of d.c component as well as an a.c. component. The presence of a.c. component is highly undesirable hence they must be eliminated from the rectifier output. **It is done by a circuit called filter.**

Fig 5.6 Filter

A filter circuit contains passive circuit elements such as inductors, capacitors, resistors and their combination. The filtering process depends upon the electrical properties of the passive circuit elements. **An inductor allows the direct current to pass through it but blocks the alternating current. A capacitor passes the alternating current but blocks the d.c. current.**

The given figure displays the concept of a filter. The output of a fullwave rectifier is given as the input of the filter. The output of the filter circuit is not exactly a constant d.c. level. It has a small amount of a.c. component which effect will be almost negligible. Therefore, **a filter circuit is a circuit which minimises the unwanted a.c. component of the rectifier output and allows only the d.c. component to reach the load.** The important filters can be listed as,

1. Inductor Filter
2. Capacitor Filter
3. Inductor - Capacitor Filter
4. π - Filter.

Inductor Filter

We used to refer it as choke filter. It has an inductor which is introduced between the rectifier ans the load resistance. The rectifier output gives a.c. components as well as d.c. components. Whenever the rectifier output passes through inductor, it passes d.c components perfectly and offers a high resistance to the a.c. components. Hence, the a.c. components

of the rectified output is filtered and d.c. component alone reaches at the load. Ideally the output of inductor filter should contain d.c voltage alone but in practice, it consists a small a.c component. The ripple factor of an inductor filter (The ripple factor can be defined as the ratio of rms value of a.c component of output voltage to the d.c. component of output voltage) is given by

$$r = \frac{R_L}{3\sqrt{2}\,\omega L} = \frac{R_L}{1330\,L}$$

Where,

r – ripple factor
R_L – Load resistance
ω – angular frequency = $2\pi f$
L – Inductor in henrys
f = 50 H z

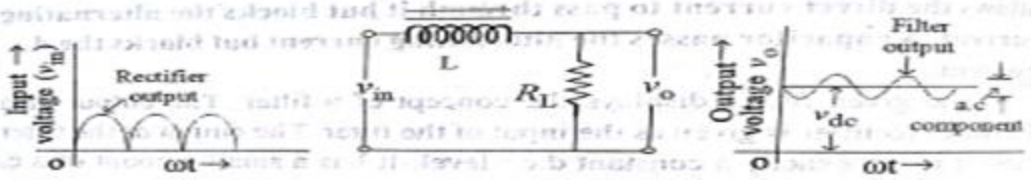


Fig 5.7 Inductor Filter

Therefore the ripple factor is proportional the load resistance and inversely proportional to the inductor. The inductor filter is more suitable for heavy load currents when the load resitance will be small. The a.c. component at the output of a filter can be decreased if we use an inductor of a large value. It is to be noted that an inductor of a high value will also have a higher d.c. resistance which makes a lower d.c. output voltage.

Capacitor Filter

Capacitor filter is an inexpensive filter for light loads (in which larger values of load resistance are required) The function of a capacitor filter is to smoothen out the voltage ripples or pulsations. The following figure displays a hlaf-wave rectifier with a capacitor filter.

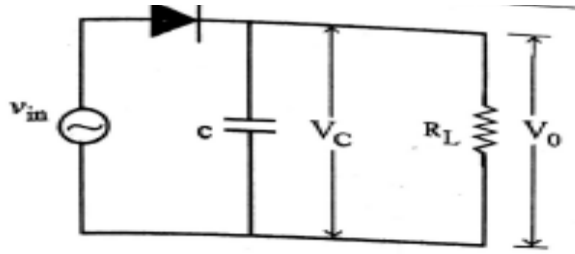


Fig. 5.8 Half - Wave rectifier with capacitor filter.

The operation of the circuit is explained in terms of the following waveforms. The first and second figures show the a.c. input voltage and the half wave rectifier output respectively. The third one shows the waveform of an filter output voltage.

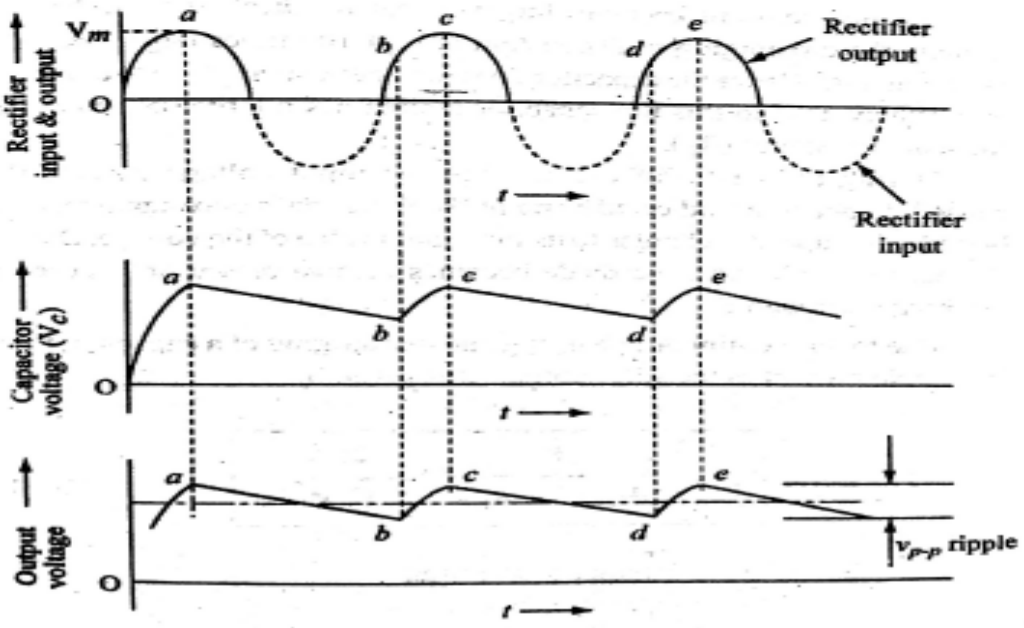


Fig 5.9 Different waveforms in a capacitor filter

While applying the positive half cycle of the a.c. input voltage, the diode is forward biased. It makes the capacitor to charge quickly to its maximum possible value of voltage (Vm). The diode forward resistance as negligible. There is no resistance in the charging path except diode forward resistance therefore the charging time is almost zero. Hence the capacitor follows the charging voltage.

As the a.c. input voltage begins to decrease below its maximum value, the capacitor returns its charge. During the negative half cycle of the input, the capacitor discharges through the load resistance as shown by the curve ab. It is to be noted that the capacitor cannot discharge through the diode because it is reverse biased. The time constant for discharging is given by,

$$T = C_0 R_L$$

As time constant becomes larges, capacitor discharge will be less. Usually the discharging time constant is kept 100 times larger than the charging time. Hence the capacitor does not have enough time to discharge appreciably. Due to this the capacitor maintaines a large voltage across the load resistance (R_L).

During the next half cycle, when the input voltage exceeds the capacitor voltage as indicated by point "b" the diode is once again forward biased. The capacitor charges to its maximum value of the voltage. During the negative half cycle the diode becomes reverse biased and capacitor discharges through R_L.

Due to the continuous charging and discharging of a capacitor, there is a ripple present at the filter output. It is given by

$$r = \frac{1}{4\sqrt{3}\, f\, C\, R_L} = \frac{2890}{C.\, R_L}$$

Where,

C – capacitance in Farads

f – frequency = 50Hz

R_L – Load resistance in ohms.

Smaller the value of this ripple will be the filtering action.

LC Filter

In an inductor filter, the riple factor is directly proportional to the load resistance. Where as, in a capacitor filter it varies inversely proportional to the load resistance. **Therefore if we combine inductor filter and capacitor filter the ripple factor will become almost independent of the load resistance.** The combination is called LC filter. The figure shows the LC filter.

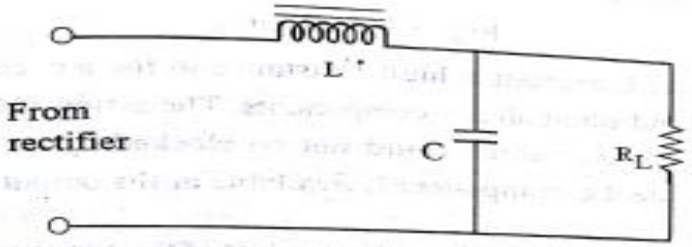


Fig. 5.10 LC filter.

The other names of LC filters are inductor input filter, choke input filter, or LC section. The ripple factor is given by

$$r = \frac{\sqrt{2}}{12\omega^2 . LC} = \frac{1.195}{LC}$$

Where L is in henrys and C in μFs.

π Filter

The filter section is appearing like letter π(pie) therefore called as π filter. It is also called capacitor input filter or CLC filter. This is used where a low output current and a high d.c. output voltage are required.

If has two capacitors C_1 and C_2 and an inductor. The pulsating output from the rectifier is given at the input teminals of the π filter. The filtering action is as follows. Capacitor C_1 allows a low reactance to a.c component of rectifier output. At the sametime it exhibits infinite resistance to the d.c component. Hence the capacitor C_1 by passes majority of a.c. component to the ground. Remaining d.c. component moves towards L.

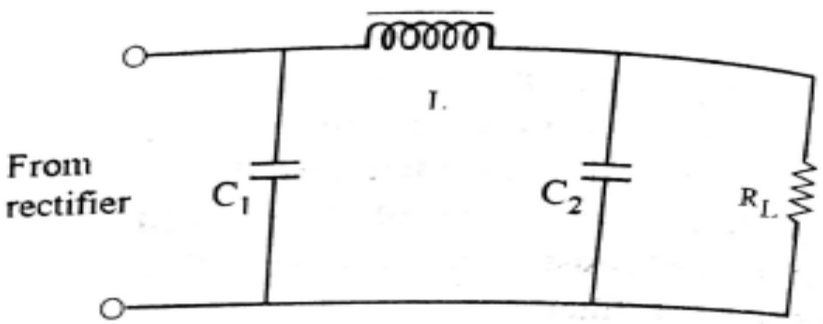


Fig. 5.11 π filter.

The inductor L exhibits a high resistance to the a.c. component of rectifier output and admit all d.c. components. The action of C_2 is similar to C_1. It by passes a.c. which could not be blocked by an inductor L. Resulting, only the d.c. component is available at the output.

The ripple factor is depends on the product of the capacitance values of C_1 and C_2. The d.c. output voltage will be high only if the value of capacitor C_1 is large. Therefore π filter will be designed with a large value of capacitor C_1.

The ripple factor of a π - filter is given by,

$$r = \frac{1}{4\sqrt{2}\,\omega^2 C_1 C_2 L R_L} = \frac{5700}{C_1 C_2 L R_L}$$

Where,

C_1, C_2 – Capacitors in Farads
L – inductor in henrys
R_L – resistance in ohms.

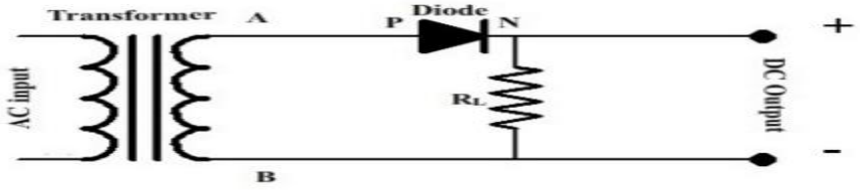
4. Explain in detail about half wave rectifier circuit and compare their performance.

Rectifier:
Rectification is the process of converting AC to DC. The circuit which is used for this purpose is known as rectifier. Rectifiers are of two types:

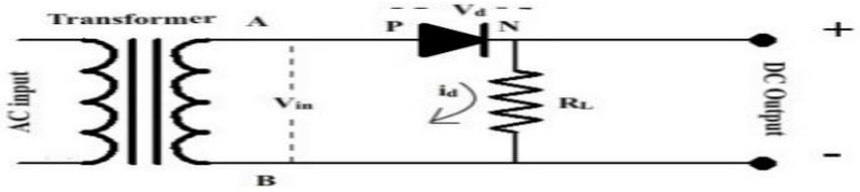
1. Half wave rectifier
2. Full wave rectifier

In a half wave rectifier, DC is available at its output terminals during one half cycle of the AC input, whereas in a full wave rectifier DC is obtained during both half cycles of the AC input.

Half wave rectifier using diode:
Assemble the half wave rectifier circuit using P-N junction diode as shown in image(1). Terminal A in the secondary is connected to the P section of the diode and the other end N is connected to B terminal through load R_L.



Image(2)



- The AC is supplied across the primary of a transformer.
- During one half of the cycle, A is positive with respect to B. This makes the P-N junction diode to conduct as it is forward biased and the current flows through the load R_L as shown in the image(2).
- During the next half cycle the point A is negative with respect to B. In this state, the diode does not conducts because it is reverse biased and hence no current passes through R_L.
- Thus current passes through the R_L only during positive cycles. Hence this circuit is known as half wave rectifier.

Using the definitions reported in the previous section, we get the following results:

$$V_{DC} = \frac{1}{T}\int_0^T v_L(t)\mathrm{d}t = \frac{1}{2\pi}\int_0^{\pi} V_S \sin(\varpi t)\mathrm{d}t = \frac{V_S}{\pi}.$$

And, similarly, we can calculate the other parameters:

$$V_L = \sqrt{\frac{1}{T}\int_0^T v_L^2(t)\mathrm{d}t} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} V_S^2 \sin^2(\varpi t)\mathrm{d}t} = \frac{V_S}{2}$$

$$I_{DC} = \frac{V_{DC}}{R_L} = \frac{V_S}{\pi \cdot R_L}$$

$$I_L = \frac{V_L}{R_L} = \frac{V_S}{2 \cdot R_L} = I_S.$$

The current in the secondary of the transformer can flow only when the diode conducts and the it is equal to the current in the load:

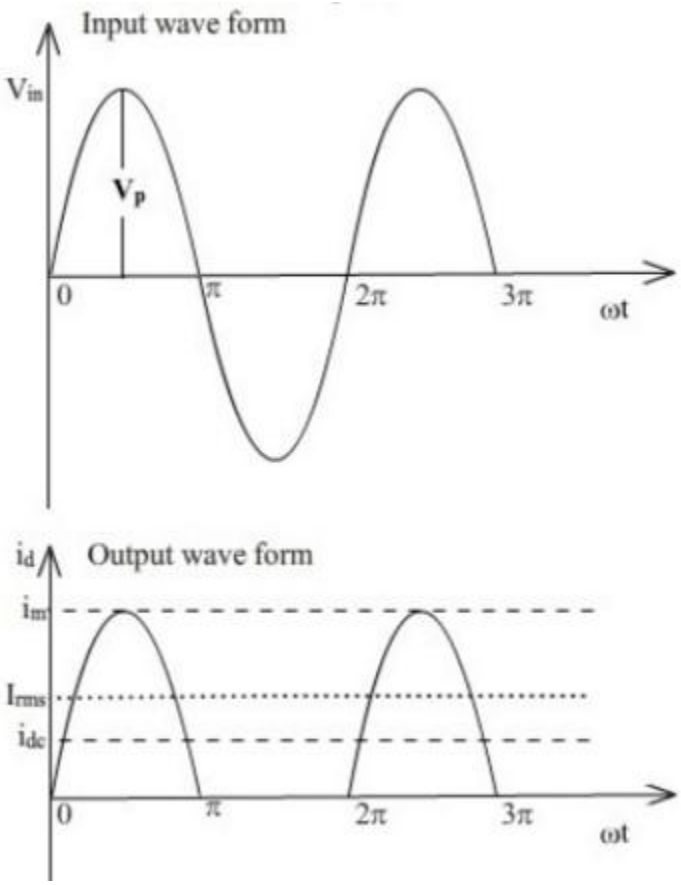
$$FF = \frac{V_L}{V_{DC}} = \frac{\pi}{2}$$

$$\eta = \left(\frac{1}{FF}\right)^2 = \frac{4}{\pi^2} = 0.405$$

$$RF = \sqrt{FF^2 - 1} = 1.21.$$

The poor performance of this rectifier is also confirmed by the utilization of the transformer. I Eq. (14), we get

$$TUF = 0.323 \text{ (or } TUF = 0.286 \text{ according to some authors).}$$



SERIES REGULATOR

The following figure shows a series op–amp regulator circuit. The essential parts of the voltage series regulator circuit are,

1. Series pass transistor
2. Reference voltage circuit
3. Error Amplifier
4. Feedback circuit.

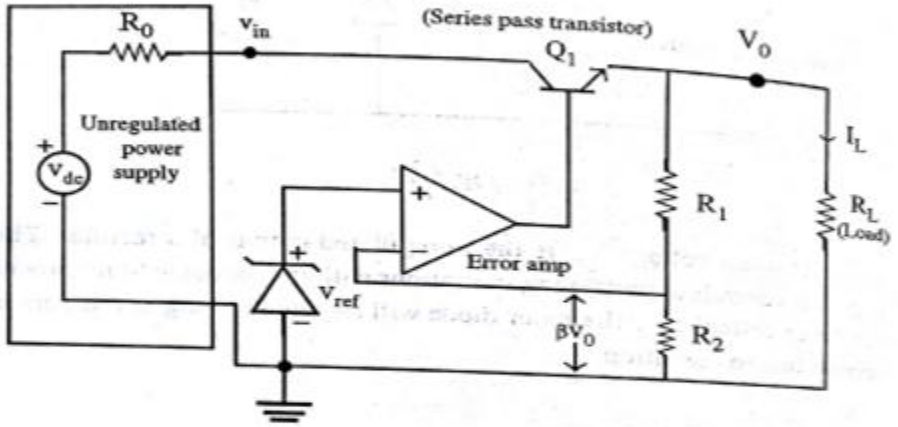


Fig 5.14 A regulated power supply

It can be observed from the diagram that power transistor is connected in series with the unregulated d.c input voltage and the regulated output voltage. Therefore it must find the difference between the two voltages for any fluctuation in output voltage. The transistor k is also connected as anemitter follower. The emitter follower offers sufficient current gain to operate the load. The output voltage has been sampled by the potential divider R_1–R_2arrangement and it is fedback to the negative input terminal of the error amplifier. The sampled output is compared with the reference voltage. The reference voltage is obtained by a zener diode. The output of the error amplifer drives the series pass transitor. Suppose the output voltage increases due to variation in load current, then the sampled voltage βV_o

also increase where, the feed back factor is decided by

$$\beta = \frac{R_2}{R_1 + R_2}$$

In turn, it reduces the output voltage of error diff–amp due to the 180° phase difference. The output of the error amplifier V_o' is vien to the base of series transitor which is used as a n emitter follower. Therefore output follows V_o' hence V_o also reduces. It implies that the increase in V_o is nullified. In a similar way, reduction in output voltage also gest nullified.

1. A linear power supply supplies constant voltage while a switched power supply doesn’t

2.A linear power supply is much simpler than a switched mode power supply

3.A switched mode power supply is more power efficient than a linear power supply

4.A switched mode power supply is more likely to create noise than a linear power supply

5. SMPs is more complex to design and needs external components like inductors and transformers.

6. SMPs is slow in responding to transient load changes compared to linear series regulator.