Bharath
INSTITUTE OF HIGHER EDUCATION AND RESEARCH
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SCHOOL OF ELECTRICAL ENGINEERING

Value Added Courses (2022 -2023)

A short term course on Advanced Digital Logic Verification

Course Objective

This course will enable the participants to Explain various IC technology options, Demonstrate Logic simulation, Design verification, Verilog.,Illustrate behavioral modeling, Boolean-Equation, Flip-Flops and Latches; multiplexers, encoders, and decoders, synchronizers for asynchronous signals.Demonstrate combinational logic; three-state devices and bus interfaces; Registered logic registers and counters; Resets; Divide and conquer: Partitioning a design and to define basics of PLA; PAL; Programmability of PLDs; CPLDs; FPGA.

Resource Persons:

1. Dr.S.Arulselvi
2. Ms.S.Aruna Mary
3. Dr.P.Dhinakar

Convener

Dr.H.Umma Habiba

HOD/ECE

Bharath Institute of Higher Education & Research Deemed to be University U/S 3 of UGC Act, 1956
Dept. of ECE

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Requisition Letter

Date: 29.12.2022

From

The HOD,
ECE Department,
Bharath Institute of Higher Education and Research,
Selaiyur, Chennai.

To
The Dean Engineering,
Bharath Institute of Higher Education and Research,
Selaiyur, Chennai.

Respected Sir,
SUB: Requisition for conducting Value Added Course-Regd

School of Electrical Engineering has planned to conduct Value added Course on "**A short term course on Advanced Digital Logic Verification"** on 18.10.2022. In this regard we kindly request you to grant permission for the same.

Thanking you

HOD/ECE

Dean Engineering

Bharath Institute of Higher Education and Research (Deemed to be University u/s 3 of the UGC Act, 1956) Dept. of ECE Chennai-73

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CIRCULAR

SCHOOL OF ELECTRICAL ENGINEERING

Date: 02.1.2023

The course on **"A short term course on Advanced Digital Logic Verification"** is planned by School of Electrical Engineering which commences on 10-1-2023(Tuesday). In this regard the students are requested to give their willingness to Course Coordinator. It is instructed to actively participate and get benefitted for the certified course.

Course Coordinator: Ms.S.Aruna Mary
Contact No: 98841181627
Email id : aruna.ece@bharathuniv.ac.in

(Dr.H.Umma Habiba)

HOD/ECE

To,
Copy to ECE Department,
Copy to EEE Department,
Department Notice Board

Dept. of ECE

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SCHOOL OF ELECTRICAL ENGINEERING

A short term course on Advanced Digital Logic Verification

SCHEDULE

Contact Hours: 31 hrs

DATE	SESSION	Contact Hours	TOPICS	Resource person
10.1.2023	FN	9.00 am to 12.30 pm	Introduction: Design methodology – An introduction; IC technology options	Mr John Thangavel
	AN	1.30 pm to 4 pm	Logic Design with Verilog: Structural models of combinational logic; Logic simulation, Design verification, and Test methodology	Ms.B. Pearly
11.1.2023	FN	9.00 am to 12.30 pm	Logic Design with Behavioral Models: Behavioral modeling; A brief look at data types for behavioral modeling;	Ms Uma Maheshswari
	AN	1.30 pm to 4 pm	RTL Design using Verilog	Ms Rekha Sharmily
12.1.2023	FN	9.00 am to 12.30 pm	Algorithmic state machine charts for behavioral modeling; ASMD charts; Behavioral models of counters, shift registers and register files;	Ms R Geetha
	AN	1.30 pm to 4 pm	Synthesis of Combinational and Sequential Logic: Introduction to synthesis; Synthesis of combinational logic;	Ms T Vanithamani
13.1.2023	FN	9.00 am to 12.30 pm	Synthesis of sequential logic with flip-flops; Synthesis of explicit state machines; Registered logic; State encoding; Synthesis of implicit state machines	Ms.I.Jeyasukumari
	AN	1.30 pm to 5 pm	Synthesis of loops; Design traps to avoid; Divide and conquer: Partitioning a design	Ms.G.Kanagavalli
18.1.2023	FN	9.00 am to 12.30 pm	Programmable Logic and Storage Devices - Introduction	Dr.P.Dhinakar
	AN	1.30 pm to 5 pm	Programmability of PLDs; CPLDs; FPGAs; Verlog-Based design flows for FPGAs; Synthesis with FPGAs.	Ms.S Aruna Mary

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VALUE ADDED COURSE

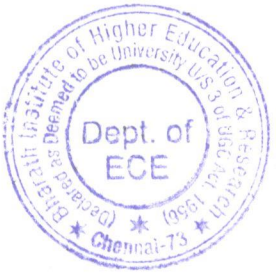
SCHOOL OF ELECTRICAL ENGINEERING

A short term course on Advanced Digital Logic Verification

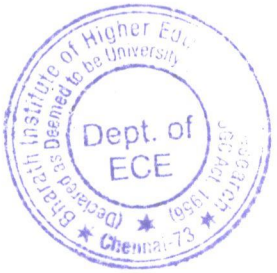
List Of Participants

Date: 18.10.2022

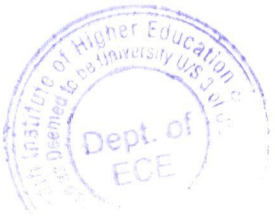
S.NO.	REG.NO	NAME
1	U21EC251	SHAIK RIZWAN BASHA
2	U21EC252	SIDDA SATYA SAI VENKATA TEJA
3	U21EC253	SIDDHARAPU PRAVEEN
4	U21EC254	SINDHIYA S
5	U21EC255	SINGAM GANGA VASUNDHAR REDDY
6	U21EC256	SINGAMSETTI LAKSHMI PRANITHA
7	U21EC257	SK ASIF
8	U21EC258	SODISETTI SIVA CHAITANYA
9	U21EC259	SUNKE ADITHYA NETHA
10	U21EC260	SUNNAMPALLI KEERTHI REDDY
11	U21EC261	SURAM YESHWANTH REDDY
12	U21EC262	SUWALA SUNAND KUMAR
13	U21EC263	SWARNA SHASHANK
14	U21EC264	SWARNA SRUTHIKA



15	U21EC265	TAMMANA LAKSHMI GANAPATHI
16	U21EC266	TANNERU SURYA
17	U21EC267	TATI KARTHIK
18	U21EC268	TEKULAPALLY ANIL
19	U21EC269	THOTA AJAY
20	U21EC270	THOTA REDDAIAH
21	U21EC271	THOTLI USHA
22	U21EC272	UPPALA ANIL
23	U21EC273	UPPALAPATI SATISH
24	U21EC274	URUTURU HARSHAVARDHAN
25	U21EC275	VADAPALLI PHANINDRA KUMAR
26	U21EC276	VAIKANTI VENKATA RAMANA
27	U21EC277	VALLAMKONDA SURESH
28	U21EC278	VALLAPUDASU VINAY KUMAR
29	U21EC279	VALLEPU ARAVIND
30	U21EC280	VANGALA SULOCHANA
31	U21EC282	VATTAM GANESH KUMAR REDDY
32	U21EC283	VATTIKONDA CHANDU
33	U21EC284	VAVILALA BADRINADH SAI
34	U21EC285	VEERAMALLA VAMSI
35	U21EC286	VEERAMREDDY SRIDHAR REDDY
36	U21EC287	VEERANKI SWARUP KUMAR
37	U21EC288	VEMULA NAVEEN
38	U21EC290	VENGALANENI RAVINDRA
39	U21EC291	VENNAPUSA UMA MAHESWAR REDDY



40	U21EC292	VIGNESH K
41	U21EC293	VIMAL SURYA S
42	U21EC294	YANAMALA HEMANTH KUMAR REDDY
43	U21EC296	YARASANI VENKATA REDDY
44	U21EC297	YASWANTH R
45	U21EC298	YEMINENI AJAY
46	U21EC299	YERRAGUNTA ANITHA
47	U21EC300	YERVA VENKATA RAMI REDDY
48	U20EC074	KOTTE SRINIVASA RAO
49	U20EC075	KUNCHAPU ARUNA
50	U20EC076	LAGA GOPICHAND
51	U20EC077	LAKKAKULA BHARATH
52	U20EC078	LAKSHMISETTY NARESH
53	U20EC079	LANKA MANICHANDRA
54	U20EC080	LAVANUR DHARANISWARA REDDY
55	U20EC081	LINGALA SIVA SHANKAR
56	U20EC082	LINGA REDDY MUKESH REDDY
57	U20EC083	LOKA VIVEK REDDY
58	U20EC084	MADANALA KARTHIK
59	U20EC085	MADU VENKATA PAVANSAI
60	U20EC086	MANAMASI ANIL
61	U20EC087	MANAMASI JAGADEESH
62	U20EC088	MANCHALA ASHOK KUMAR REDDY
63	U20EC089	MANDATI YASWANTH
64	U20EC091	A MANIDEEP



65	U20EC092	MANNALA DEVENDRA VARAPRASAD
66	U20EC093	MARELLA VISHNU
67	U20EC094	MARKA SIDDU
68	U20EC095	MIDDE VENKATESWARARAO
69	U20EC096	MOLAKA SRI RAVEENDRA
70	U20EC097	MORUSU JITHENDRA
71	U20EC098	MOTHUKURI CHARAN SANKAR
72	U20EC099	MOVVA SWECHHA BHAVANI
73	U20EC100	MUMMA REDDY THARUN TEJA
74	U20EC101	MYLA RAMU
75	U20EC102	NAGABHAIRU VENKATAPAVANKUMAR

(Dr.H.Umma Habiba)

HOD/ECE

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FEED BACK FORM		Date:18.1.2023			
Name	Myla Ramu				
Register number	U2OECI01				
	Poor	Fair	Good	Very Good	Excellent
Overall Program					✓
TheSpeaker					✓
Audio,Visual Aids Technology used					✓
Presentation hand outs					✓

Dept. of ECE

Student Signature

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VALUE ADDED COURSE

A short term course on Advanced Digital Logic Verification

FEED BACK FORM	Date 18.01.2023				
Name	Yaswanth.R				
Register number	U21EC297				
	Poor	Fair	Good	Very Good	Excellent
Overall Program				✓	
TheSpeaker				✓	
Audio,Visual Aids Technology used					✓
Presentation hand outs					✓

Student Signature

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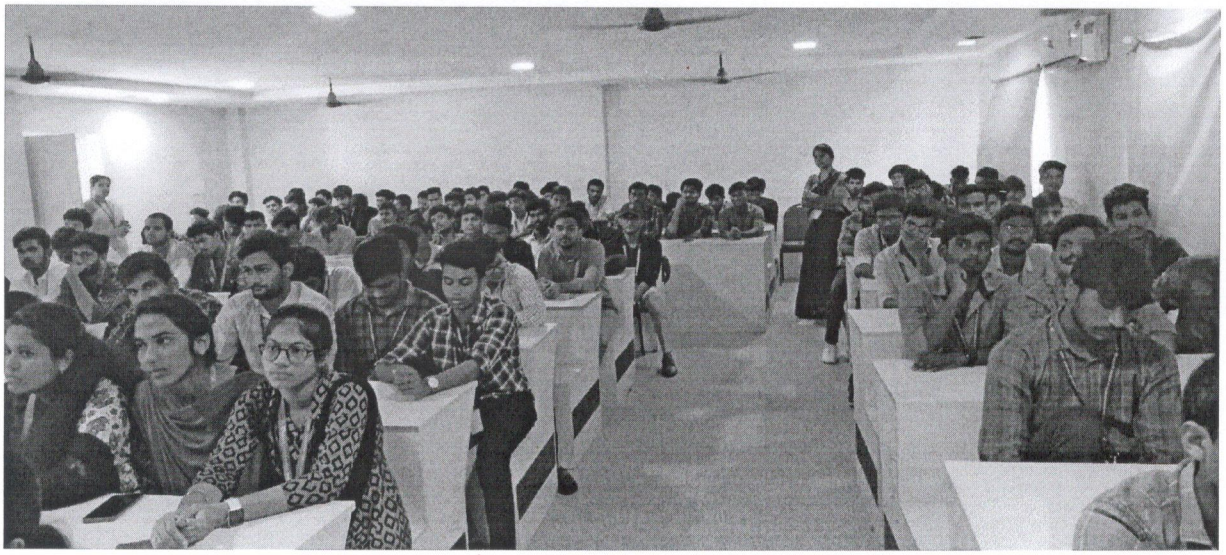
SCHOOL OF ELECTRICAL ENGINEERING

Course on "A short term course on Advanced Digital Logic Verification" dated on 10.1.2023 conducted by school of Electrical Engineering



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SCHOOL OF ELECTRICAL ENGINEERING

CERTIFICATE OF PARTICIPATION

This is to certify that Mr/Ms. TAMMANA LAKSHMI GANAPATHI has attended Values added Course on "**A short term course on Advanced Digital Logic Verification** " Organized by the school of Electrical Engineering, BIHER conducted from 10.01.2023 to 18-01-2023.

Ms. S. ARUNA MARY
COURSE COORDINATOR

Dr. H.UMMA HABIBA
CONVENOR