Bharath
INSTITUTE OF HIGHER EDUCATION AND RESEARCH
Declared as Deemed-to-be-University u/s 3 of the UGC Act, 1956

SCHOOL OF ELECTRICAL ENGINEERING

Innovations in processor Architecture

Value Added Course-2017

Course Objective

The objective of this course of study is to provide students with a glimpse into the semiconductor industry that has been the foundation upon which the electronics industry has been based for the past half century, and to provide insight into the future of that industry as well as nanotechnology in general. In the last 50 years, the dimensions of the features built into integrated circuits have shrunk from 25 mm to 25 nm. Over the next decade these features will approach atomic dimensions, giving rise to a host of unique nanotechnology challenges and opportunities.

The definition and description of the terminology and processes of microelectronics; semiconductor facilities and chemical processes for integrated circuit manufacture with an emphasis upon unit processes; the major unit processes including thin-film metal and dielectric deposition and etching, silicon oxidation and etching, ion implantation, diffusion, lithography, and planarization; an overview of promising nano patterning and nanofabrication techniques, such as electron and other particle-beam imaging, nanoimprint, and near-field probe imaging.

Resource Persons :

1.Ms.S.Saravana

2.Ms.K.Subbulakshmi

3.Ms.B.Hemalatha

Convener

Dr.M.Sangeetha

HOD/ECE

INSTITUTE OF HIGHER EDUCATION AND RESEARCH DEPT of ECE Chennai-73

Bharath
INSTITUTE OF HIGHER EDUCATION AND RESEARCH
Declared as Deemed-to-be-University u/s 3 of the UGC Act, 1956

CIRCULAR

SCHOOL OF ELECTRICAL ENGINEERING

Date: 01.11.2017

The course on Innovations in processor Architecture is planned by School of Electrical Engineering which commences on 27.11.2017(Monday). In this regard the students are requested to give their willingness to Course Coordinator. It is instructed to actively participate and get benefitted for the certified course.

Course Coordinator: M. Sowmiya Manoj
Contact No:7358747803
Email id : sowmiyamanoj.ece@bharathuniv.ac.in

(Dr.M.Sangeetha)
HOD/ECE

DEPT of ECE

To,
Copy to ECE Department,
Copy to EEE Department,
Department Notice Board

Bharath
INSTITUTE OF HIGHER EDUCATION AND RESEARCH
Declared as Deemed-to-be-University u/s 3 of the UGC Act, 1956

SCHOOL OF ELECTRICAL ENGINEERING

Innovations in processor Architecture

SCHEDULE

Contact Hours : 32 hrs

DATE	SESSION	Contact Hours	TOPICS	Resource person
27.11.2017	FN	9.00 am to 12.30 pm	Organization of the von Neumann machine; Instruction formats; Pipeline - fetch/execute cycle, Instruction decoding and execution; Registers and register files; Instruction types and addressing modes; Subroutine call and return mechanisms; Other design issues	Ms.B.Hemalatha
	AN	1.30 pm to 4 pm	Data Representation, Hardware and software implementation of arithmetic unit for common arithmetic operations: addition, subtraction	Ms.S.Saravana
28.11.2017	FN	9.00 am to 12.30 pm	multiplication, division(Fixed point and floating point)-floating point IEEE standards	Ms.B.Hemalatha
	AN	1.30 pm to 4 pm	Conversion between integer and real numbers- rounding and truncation; The generation of higher order functions from square roots to transcendental functions; Representation of non-numeric data (character codes, graphical data)	Ms.K.Subbulakshmi
29.11.2017	FN	9.00 am to 12.30 pm	Memory systems hierarchy; Coding, data compression, and data integrity;	Ms.S.Saravana

			Electronic, magnetic and optical technologies; Main memory organization, Types of Main memories, and its characteristics and performance;	
	AN	1.30 pm to 4 pm	Organization of the von Neumann machine; Instruction formats; Pipeline - fetch/execute cycle, Instruction decoding and execution; Registers and register files; Instruction types and addressing modes; Subroutine call and return mechanisms; Other design issues	Ms.K.Subbulakshmi
30.11.2017	FN	9.00 am to 12.30 pm	Latency, cycle time, bandwidth, and interleaving; Cachememories (address mapping, line size, replacement and write-back policies)	Ms.B.Hemalatha
	AN	1.30 pm to 5 pm	Virtual memory systems-paging, segmentation, address mapping, page tables, page replacement algorithms; Reliability of memory systems; error detecting and error correcting systems	Ms.S.Saravana
01.12.2017	FN	9.00 am to 12.30 pm	I/O fundamentals: handshaking, buffering; I/O techniques: programmed I/O, interrupt-driven I/O, DMA; Buses: bus protocols, local and geographic arbitration. Interrupt structures: vectored and prioritized, interrupt overhead, interrupts and reentrant code	Ms.K.Subbulakshmi
	AN	1.30 pm to 5 pm	External storage systems; organization and structure of disk drives and optical memory; Flashmemories, Basic I/O controllers such as a keyboard and a mouse;RAID architectures; I/O Performance; SMART technology and fault detection	Ms.S.Saravana

VALUE ADDED COURSE

SCHOOL OF ELECTRICAL ENGINEERING

Innovations in processor Architecture

List Of Participants

Date:27.11.2017

Sl.no	REG.NO	NAME OF THE CANDIDATE
1	U14EC001	AAKAASH THAKUR
2	U14EC004	K ABHILASH REDDY
3	U14EC006	ADDUGALA RAMA DEVI
4	U14EC007	ADHARSH.A .I
5	U14EC008	ADIREDDY PRAVEEN
6	U14EC010	AMARJEET KUMAR
7	U14EC016	ARCHANA.R
8	U14EC017	ASARA ANITH RAO
9	U14EC018	BANKIM CHANDRA BHARTI
10	U14EC019	BEDDINTI PRAVEEN KUMAR
11	U14EC022	BOYAPATI PUSHYAMITHRA
12	U14EC024	CHANDRALEKA.K
13	U14EC025	CHEKURI.VENKATA MAHESH
14	U14EC026	CHINTA ANVESH
15	U14EC028	DEBAJIT HAZARIKA
16	U14EC035	DUVVURU SREENIVASA TEJA
17	U14EC036	EJJAGIRI PRAVEEN
18	U14EC037	VIJAYA LAKSHMI EJJI

19	U14EC040	GARAGA SIVA SURYA DEEPAK
20	U14EC043	GOVINDUGARI NITHIN REDDY
21	U14EC044	GUJJARI SHIVADURGA PRASAD
22	U14EC045	GULAM AHMED REJA
23	U14EC050	KATHA HARSHA VARDHAN REDDY
24	U14EC052	JERALD.M.S
25	U14EC053	KAKARAPARTHY CHITRA HARSHAN
26	U14EC056	KALAI ARASI.M
27	U14EC058	KAMIREDDY SAI VEERA LAKHSMI MONIKA
28	U14EC059	KANALA RAMANJANEYA REDDY
29	U14EC070	KONDA MOHITH KUMAR REDDY
30	U14EC071	KONDURI SURENDRAREDDY
31	U14EC072	KONDURU PAVAN SAI
32	U14EC073	KOTA VIDYA SAGAR
33	U14EC078	MANNEM MAHANTH REDDY
34	U14EC080	MARKA RAJ KUMAR
35	U14EC082	MD.FAIYAZ ALAM
36	U14EC087	MOLABANTI SAI KARTHIK
37	U14EC088	VASIREDDY MOUNIKA.
38	U14EC089	MUDRAKOLLA SURESH SACHIN
39	U14EC090	MUTYALA SAI HARISHITHA
40	U14EC098	NILKAMAL KUMAR
41	U14EC099	PADALA SUBRAHMANYAM
42	U14EC100	PALAPARTHI RAMBABU
43	U14EC107	PILLI DANIEL PHILIP MOSES

44	U14EC108	PONNAGANTI MANOJ DEEP
45	U14EC109	G PRANAY KUMAR
46	U14EC116	KAKUMANU RADHA RANI
47	U14EC117	PAWAR.SUSHEEL KUMAR
48	U14EC139	SRIRAMULA PRANAV
49	U14EC140	SUSHEEL RANJAN
50	U14EC141	SWETHA HARIDASAN
51	U14EC148	THILLAI VANI.S
52	U14EC149	THIRUVATTURU HARIKRISHNA
53	U14EC158	VANGALA.CHANDRA SEKHAR REDDY
54	U14EC162	BUKAI VENKATESH NAIK.
55	U14EC165	VISWANATHAN.B
56	U14EC166	VONDANA TARAKESHWAR RAO

(Dr.M.Sangeetha)

HOD/ECE

DEPT of ECE

Bharath
INSTITUTE OF HIGHER EDUCATION AND RESEARCH
Declared as Deemed-to-be-University u/s 3 of the UGC Act, 1956

SCHOOL OF ELECTRICAL ENGINEERING

Course on **Innovations in processor Architecture** dated on 27.11.2017 conducted by School of Electrical Engineering

Bharath

INSTITUTE OF HIGHER EDUCATION AND RESEARCH

(Declared as Deemed - to - be - University under section 3 of UGC Act 1956)

NAAC

ABET

SCHOOL OF ELECTRICAL ENGINEERING

CERTIFICATE OF PARTICIPATION

This is to certify that Mr / Ms **CHINTA ANVESH(U14EC026)** has attended Value added Course On ***"Innovations In Processor Architecture"*** organized by the School of Electrical Engineering, BIHER conducted from 27-11-2017 to 01-12-2017.

M.SOWMIYA MANOJ
COURSE COORDINATOR

Dr.M.SANGEETHA
CONVENOR

Bharath
INSTITUTE OF HIGHER EDUCATION AND RESEARCH
Declared as Deemed-to-be-University u/s 3 of the UGC Act, 1956

SCHOOL OF ELECTRICAL ENGINEERING

VALUE ADDED COURSE

Innovations in processor Architecture

FEED BACK FORM				Date: 1/12/17	
Name	Kota Vidya Sagar.				
Register number	U14EC073				
Phone number	9123467781				
Email address	Vidya1234@gmail.com				
	Poor	Fair	Good	Very Good	Excellent
Overall Program				✓	
TheSpeaker					✓
Audio,Visual Aids Technology used		✓		✓	
Presentation hand outs					✓

Kotha Vidya Sagar.

Student Signature

Bharath
INSTITUTE OF HIGHER EDUCATION AND RESEARCH
Declared as Deemed-to-be-University u/s 3 of the UGC Act, 1956

SCHOOL OF ELECTRICAL ENGINEERING

VALUE ADDED COURSE

Innovations in processor Architecture

FEED BACK FORM					Date: 1/12/17
Name	Lins Rexine D				
Register number	U14EE704				
Phone number	7358179091				
Email address	Lins2010@gmail.com				
	Poor	Fair	Good	Very Good	Excellent
Overall Program				✓	
TheSpeaker					✓
Audio,Visual Aids Technology used				✓	
Presentation hand outs					✓

Student Signature