SCHOOL OF ELECTRICAL ENGINEERING

Value Added Courses (2021 -2022)

Introduction to FPGA Design for Embedded Systems

Course Objective

The major objective of this course is FPGA design in Embedded Systems along with practical design aids. The FPGA is the technology for embedded system development. The various design factors such as selection of the best FPGA architecture for a given application, how to use state of the art software tools for FPGA development, and solve critical digital design problems using FPGAs are focused in this course. The FPGA development tools are used to complete several example designs, including a custom processor. The latest software and FPGA development tools and hardware platforms to help develop a broad perspective of the capabilities of various Programmable SoC solutions are focused in this course.
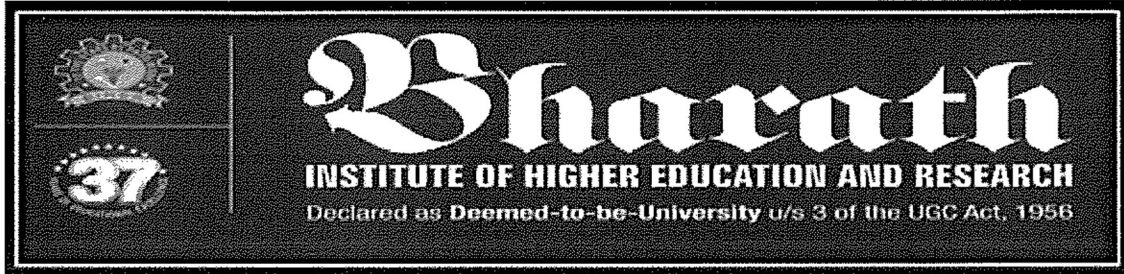
Resource Persons:

1. Ms. S. Arulselvi

2. Ms. Beulah Hemalatha

3. Ms. G. Kanagavalli

Convener

Dr.M.Sundararajan

HOD/ECE

CIRCULAR
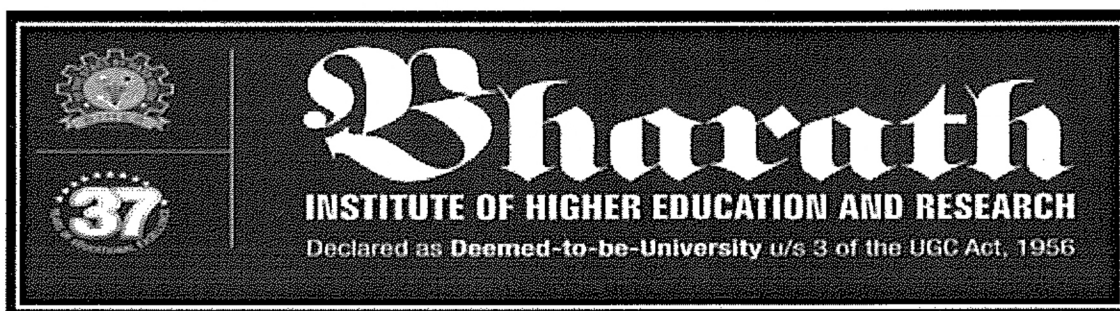
SCHOOL OF ELECTRICAL ENGINEERING

Date:20.09.2021

The course on Introduction to FPGA Design for Embedded Systemsplanned by School of Electrical Engineering which commences on 17-10-2021 .In this regard the students are requested to give their willingness to Course Coordinator.It is instructed to actively participate and get benefitted for the certified course.

Course Coordinator:Ms. S. Arulselvi
Contact No:8870334286
Email id:arulselvi.ece@bharathuniv.ac.in

(Dr.M.Sundararajan)

HOD/ECE

To,
Copy to ECE Department,
Copy to EEE Department,
Department Notice Board

SCHOOL OF ELECTRICAL ENGINEERING

Introduction to FPGA Design for Embedded Systems

SCHEDULE

Contact Hours: 30hrs

DATE	SESSION	Contact Hours	TOPICS	Resource person
17-10-2021	FN	9.00 am to 12.30 pm	Introduction to FPGA Design for Embedded Systems	Ms. S. Arulselvi
	AN	1.30 pm to 4 pm	Introduction to Hardware Description Languages	Ms. G. Kanagavalli
18-10-2021	FN	9.00 am to 12.30 pm	Hardware Description Languages for FPGA Design	Ms. Beulah Hemalatha
	AN	1.30 pm to 4 pm	FPGA Softcore Processors	Ms. S. Arulselvi
19-10-2021	FN	9.00 am to 12.30 pm	Software-hardware integration	Ms. Beulah Hemalatha
	AN	1.30 pm to 4 pm	Embedded software Use of soft-core processors	Ms. S. Arulselvi
20-10-2021	FN	9.00 am to 12.30 pm	Embedded software Use of hard-core processors	Ms. G. Kanagavalli
	AN	1.30 pm to 4 pm	OS options FPGA System	Ms. Beulah Hemalatha
21-10-2021	FN	9.00 am to 12.30 pm	Building FPGA Projects	Ms. S. Arulselvi
	AN	1.30 pm to 4 pm	Building FPGA based Embedded projects	Ms. G. Kanagavalli

VALUE ADDED COURSE

SCHOOL OF ELECTRICAL ENGINEERING

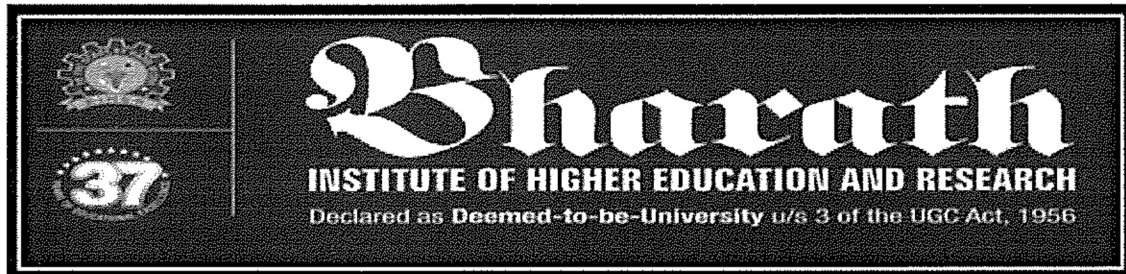### Introduction to FPGA Design for Embedded Systems

List Of Participants

Date:17.10.2021

Sl.no	REG.N0.	NAME OF THE CANDIDATE
1	U13EC001	ABINAYA P
2	U13EC002	AKHIRUL ISLAM
3	U13EC003	ANAND RAHUL
4	U13EC004	ANGEL M
5	U13EC005	ANJALI KUMARI
6	U13EC006	ARAVIND V
7	U13EC008	ASHIQUE ALAM
8	U13EC009	ASHVATHAMAN K
9	U13EC010	BABLOO KUMAR
10	U13EC011	BALRAM YADAV
11	U13EC012	CLIFFORD JOSEPH A
12	U13EC013	DAMODARAN M
13	U13EC014	DEEPAK KUMAR
14	U13EC015	DEEPAN R
15	U13EC016	DEEPSHIKHA KUMARI
16	U13EC017	DEVENDRA PRIYANKA SUNDER
17	U13EC018	ELVIS RYNTONG
18	U13EC019	G RAHUL REDDY

19	U13EC020	ISWARYA S
20	U13EC021	JAYED AHMED LASKAR
21	U13EC023	KUMARI PRIYANKA
22	U13EC024	MD ANIS
23	U13EC025	MURALITHARAN N
24	U13EC026	NABIL NAIDU S
25	U13EC027	NADAR PAVITRA KESHAVAN
26	U13EC028	NAVEEN KANNAN N
27	U13EC029	NIRAJ KUMAR
28	U13EC030	P PRAVEEN
29	U13EC031	PRAVEEN KUMAR V
30	U13EC032	RAHUL KUMAR
31	U13EC033	RAKESH V
32	U13EC034	RAMYA S
33	U13EC035	RAVIKANT SINGH
34	U13EC036	SAGNATI VAISHNU VERMA RAJU
35	U13EC038	SHRUTHI T S
36	U13EC039	SHUBHAM KUMAR
37	U13EC040	SUKANTO SHARAN
38	U13EC041	THIYAGARAJAN V
39	U13EC042	UTTAM KUMAR
40	U13EC043	VARSHA KUMARI
41	U13EC044	VIJAYKIRAN J
42	U13EC045	VIVEKANAND SINGH
43	U13EC046	YAMINISHA K

| 44	U13EC047	ZAHID AHMED
45	U13EC048	BHUVANAPRIYA R
46	U13EC049	RITESH KUMAR
47	U13EC051	LAICHIMA BRAHMA
48	U13EC052	ARUN K
49	U13EC053	VASU DHEVAN K
50	U13EE503	RAMKUMAR. R
51	U13EE504	JESS DIVYAN.P
52	U13EE505	CHAITANYA.R.G.S

Dr.M.Sundararajan
HOD/ECE

SCHOOL OF ELECTRICAL ENGINEERING

Course on Introduction to FPGA Design for Embedded Systemsdated on 17.10.2021 conducted by School of Electrical Engineering
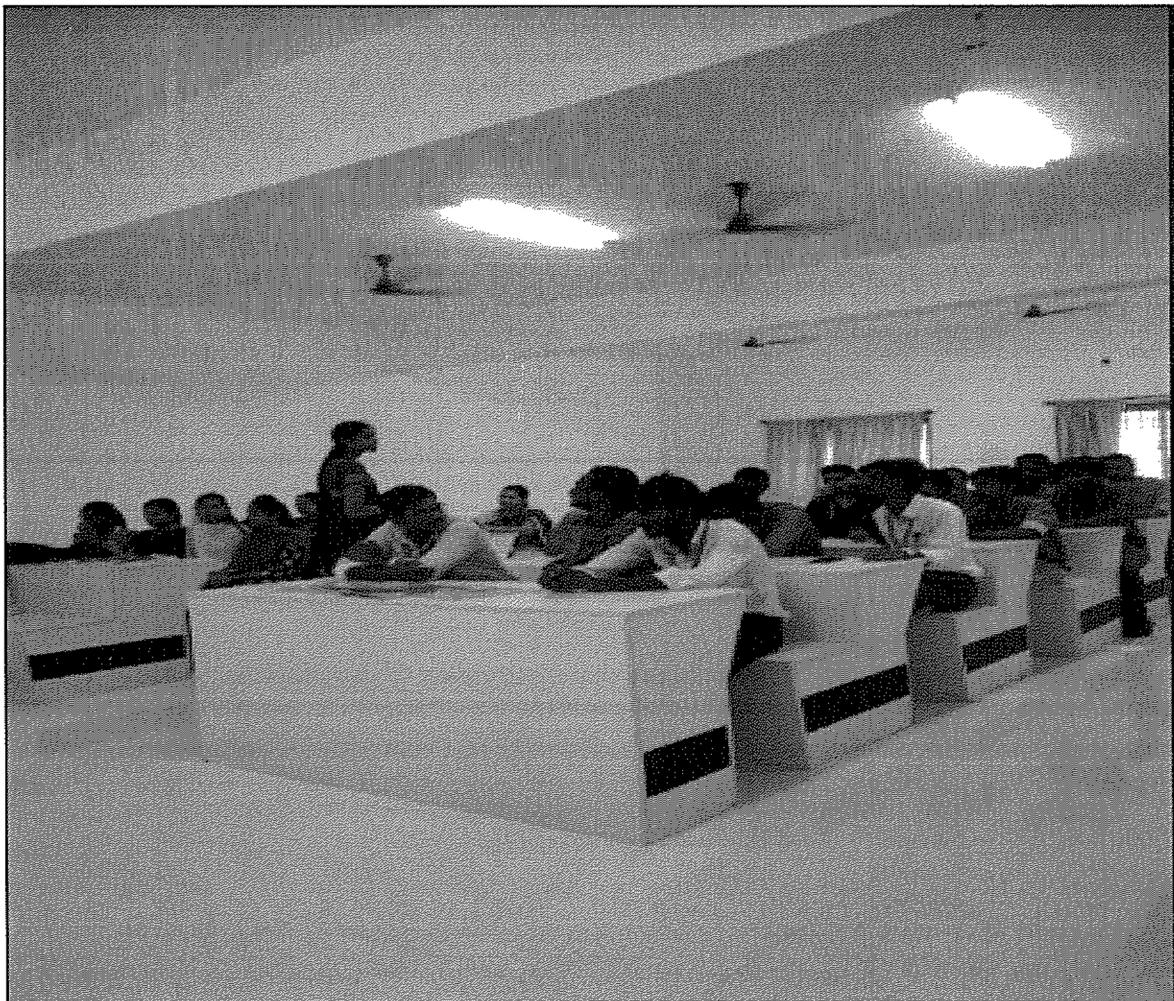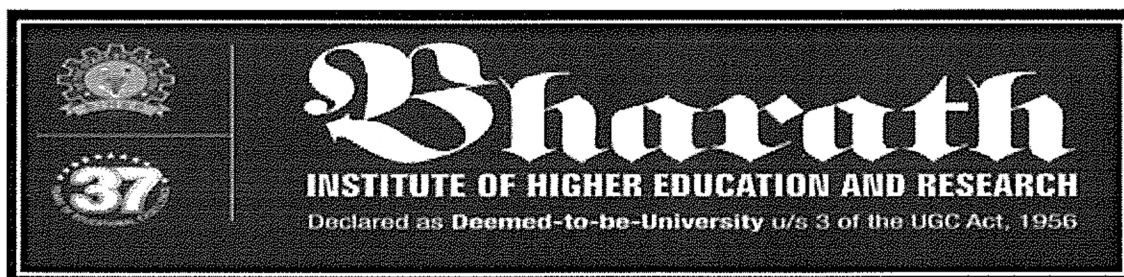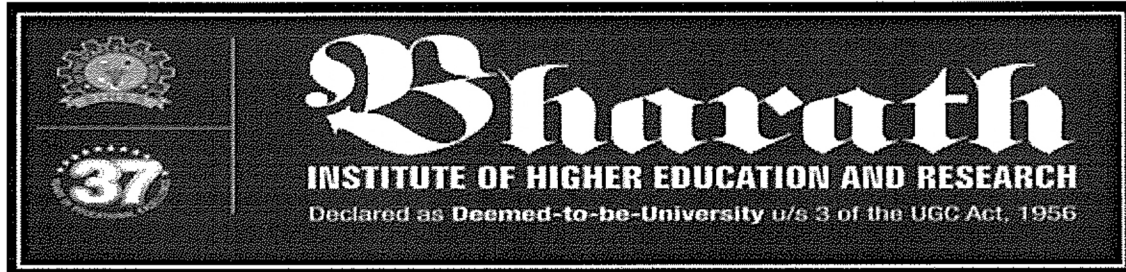
SCHOOL OF ELECTRICAL ENGINEERING

VALUE ADDED COURSE

Introduction to FPGA Design for Embedded Systems

FEED BACK FORM				Date:21/10/2021	

| Name	ARAVIND .V				
Register number	U I3 EC006				
Phonenumber	9444353565				
Email address	aravindv123@ gmail. com .				
	Poor	**Fair**	**Good**	**Very Good**	**Excellent**
Overall Program			✓		
TheSpeaker				✓	
Audio,Visual Aids Technology used					✓
Presentation hand outs			✓		

Student Signature

SCHOOL OF ELECTRICAL ENGINEERING

VALUE ADDED COURSE

Introduction to FPGA Design for Embedded Systems

FEED BACK FORM				Date:21/10/2021	

Name	RAM KUMAR. R				
Register number	U13EE503				
Phonenumber	9944707600				
Email address	Kumar. eee@ gmail.com				
	Poor	Fair	Good	Very Good	Excellent
Overall Program				✓	
TheSpeaker					✓
Audio,Visual Aids Technology used			✓		
Presentation hand outs					✓

Ram Kumar

Student Signature

Bharath
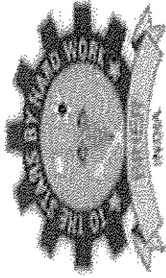
INSTITUTE OF HIGHER EDUCATION AND RESEARCH
(Declared as Deemed - to - be - University under section 3 of UGC Act 1956)

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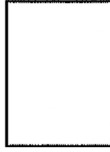
SCHOOL OF ELECTRICAL ENGINEERING

CERTIFICATE OF PARTICIPATION

This is to certify that Mr/Ms.............. **ANAND RAHUL (U13EC003)**

has attended Value added Course on **"Introduction to FPGA Design for Embedded Systems"** Organized by the school of Electrical Engineering,

BIHER conducted from 17-10-2021 to 21-10-2021.

Ms. S. ARULSELVI
COURSE COORDINATOR

Dr. M. SUNDARARAJAN
CONVENOR