Bharath
INSTITUTE OF HIGHER EDUCATION AND RESEARCH
Declared as Deemed-to-be-University u/s 3 of the UGC Act, 1956

Requisition Letter **Date: 12.06.2018**

From

The HOD,
ECE Department,
Bharath Institute of Higher Education and Research,
Selaiyur,Chennai.

To
The Dean Engineering,
Bharath Institute of Higher Education and Research,
Selaiyur,Chennai.

Respected Sir,

SUB : Requisition for conducting Value Added Course-Regd

School of Electrical Engineering has planned to conduct Value added Course on"Mapping Signal Processing Algorithms To Architectures " on 22.04.2019. In this regard we kindly request you to grant permission for the same.

Thanking you

HOD/ECE

DEPT of ECE

Dean Engineering

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CIRCULAR

SCHOOL OF ELECTRICAL ENGINEERING

Date: 02.04.2019

The course on Mapping Signal Processing Algorithms To Architectures is planned by School of Electrical Engineering which commences on 22-4-2019(Monday).In this regard the students are requested to give their willingness to Course Coordinator. It is instructed to actively participate and get benefitted for the certified course.

Course Coordinator: S.Balaji
Contact No:9566078080
Email id : balajis.ece@bharathuniv.ac.in

(Dr.M.Sangeetha)
HOD/ECE

DEPT of ECE

To,
Copy to ECE Department,
Copy to EEE Department,
Department Notice Board

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SCHOOL OF ELECTRICAL ENGINEERING

Value Added Courses (2018 -2019)

Mapping Signal Processing Algorithms To Architectures

Course Objective

Digital Signal Processing typically involves repetitive computations being performed on streams of input data, subject to constraints such as sampling rate or desired throughput. Often such systems need to be implemented under tight constraints on factors such as timing, resources, power or cost. When they are used in embedded systems, it is often worth the effort to design custom architectures that have much better cost tradeoffs than general purpose computing architectures. This course deals with the analysis of such algorithms, and mapping them to architectures that are either custom designed or have specific extensions that make them better suited to certain kinds of operations. Topics covered include fundamental bounds on performance, mapping to dedicated and custom resource shared architectures, and techniques for automating the process of scheduling. Aspects of architectures such as memory access, shared buses, and memory mapped accelerators will be studied. Assignments will cover various aspects of the design process, starting from implementing and testing specifications, to synthesis and scheduling using high level synthesis tools, and analyzing and improving the resulting architectures.

Resource Persons :

1.Hemalatha B

2.Sowmiya Manoj .M

Convener

Dr.M.Sangeetha

HOD/ECE

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Mapping Signal Processing Alogorithms To Architectures

SCHEDULE

Contact Hours : 32 hrs

DATE	SESSION	Contact Hours	TOPICS	Resource person
22-4-2019	FN	9.00 am to 12.30 pm	Digital systems, DSP, computer architecture	Hemalatha B
	AN	1.30 pm to 4 pm	DSP system models; quality metrics and bounds; number representations	Sowmiya Manoj .M
23-4-2019	FN	9.00 am to 12.30 pm	Implementation: dedicated hardware; transforms; resource sharing;	Hemalatha B
	AN	1.30 pm to 4 pm	Architectures: programmable systems; FSMs and microprograms;	Sowmiya Manoj .M
24-4-2019	FN	9.00 am to 12.30 pm	Memory and communication systems: bus structures; DMA; networks-on-chip	Hemalatha B
	AN	1.30 pm to 4 pm	Specialized architectures: Systolic arrays;	Sowmiya Manoj .M
25-4-2019	FN	9.00 am to 12.30 pm	Scheduling: time and resource bounds; allocation	Hemalatha B
	AN	1.30 pm to 5 pm	instruction extensions; peripheral accelerators	Sowmiya Manoj .M
26-4-2019	FN	9.00 am to 12.30 pm	binding, scheduling,techniques	Hemalatha B
	AN	1.30 pm to 5 pm	CORDIC; GPU	Sowmiya Manoj .M

VALUE ADDED COURSE

SCHOOL OF ELECTRICAL ENGINEERING

Mapping Signal Processing Algorithms To Architectures

List Of Participants

Date: 22-4-2019

Sl.No	REG.N0	NAME OF THE CANDIDATE
1	U14EC001	AAKAASH THAKUR
2	U14EC002	AARTHI.P
3	U14EC003	ABBISETTY SAI NIHARIKA
4	U14EC004	K ABHILASH REDDY
5	U14EC006	ADDUGALA RAMA DEVI
6	U14EC007	ADHARSH.A .I
7	U14EC008	ADIREDDY PRAVEEN
8	U14EC010	AMARJEET KUMAR
9	U14EC011	R AMULYA
10	U14EC012	MAHAMKALI VENKATA SAI NANDAANIRUDH.
11	U14EC013	ANKIT KAUSHAL
12	U14EC014	ANNAPANENI VAMSIDHAR
13	U14EC015	ANUSHA.R
14	U14EC016	ARCHANA.R
15	U14EC017	ASARA ANITH RAO
16	U14EC018	BANKIM CHANDRA BHARTI

17	U14EC019	BEDDINTI PRAVEEN KUMAR
18	U14EC020	BETHALA MOURYA
19	U14EC021	BOJJA. VENKATA PRASAD
20	U14EC022	BOYAPATI PUSHYAMITHRA
21	U14EC023	CHALUVADI DIVYA BHARATHI
22	U14EC024	CHANDRALEKA.K
23	U14EC025	CHEKURI.VENKATA MAHESH
24	U14EC026	CHINTA ANVESH
25	U14EC027	DAMMALAPATI RAHUL DIVYESH
26	U14EC028	DEBAJIT HAZARIKA
27	U14EC029	DEENADHAYALAN.A
28	U14EC030	DEEPAK KUMAR
29	U14EC031	DEEPAK.A
30	U14EC032	DESHI VENKATESH
31	U14EC033	N DHEERAJ
32	U14EC034	DOLLY NISHA J.S.
33	U14EC035	DUVVURU SREENIVASA TEJA
34	U14EC036	EJJAGIRI PRAVEEN
35	U14EC037	VIJAYA LAKSHMI EJJI
36	U14EC038	GADDI TEJA RAM
37	U14EC039	GADE MALLA REDDY
38	U14EC040	GARAGA SIVA SURYA DEEPAK
39	U14EC041	S GOKUL
40	U14EC042	GOURU VENKATA SAI PRAKASH
41	U14EC043	GOVINDUGARI NITHIN REDDY

42	U14EC044	GUJJARI SHIVADURGA PRASAD
43	U14EC001	AAKAASH THAKUR
44	U14EC002	AARTHI.P
45	U14EE001	ABENASH.R
46	U14EE002	ABHISHEK KUMAR
47	U14EE003	AJAY KUMAR MISHRA
48	U14EE004	AJMEERA. SWAPNA

(Dr.M.Sangeetha)

HOD/ECE

BHARATH INSTITUTE OF HIGHER EDUCATION AND RESEARCH
DEPT of ECE
Chennai-73

Bharath

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NAAC

ABET

SCHOOL OF ELECTRICAL ENGINEERING

CERTIFICATE OF PARTICIPATION

This is to certify that Mr / Ms **ABBISETTY SAI NIHARIKA(U14EC003)** has attended Value added Course On **"Mapping Signal Processing Alogorithms To Architectures"** organized by the School of Electrical Engineering, BIHER conducted from 22-4-2019 to 26-4-2019.

S. Balaji

BALAJI S
COURSE COORDINATOR

Dr.M.SANGEETHA
CONVENOR

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Mapping Signal Processing Algorithms To Architectures

FEED BACK FORM				Date:26-4-2019	
Name	BHANKIM CHANDRA BHARATHI				
Register number	U14EC018				
	Poor	Fair	Good	Very Good	Excellent
Overall Program				✓	
TheSpeaker					✓
Audio,Visual Aids Technology used				✓	
Presentation hand outs					✓

Student Signature

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VALUE ADDED COURSE

Mapping Signal Processing Algorithms To Architectures

FEED BACK FORM				Date:26-4-2019	
Name	ABHISHEK KUMAR				
Register number	15EE002				
	Poor	Fair	Good	Very Good	Excellent
Overall Program				✓	
TheSpeaker				✓	
Audio,Visual Aids Technology used					✓
Presentation hand outs					✓

Student Signature

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Course on Mapping Signal Processing Algorithms To Architectures dated on 22-4-2019 conducted by school of Electrical Engineering