Bharath
INSTITUTE OF HIGHER EDUCATION AND RESEARCH
Declared as Deemed-to-be-University u/s 3 of the UGC Act, 1956

SCHOOL OF ELECTRICAL ENGINEERING

Value Added Courses (2020 -2021)

Advanced Digital Logic Verification(Online)

Course Objective

This certification helps you develop skills required to become a verification engineers. It covers writing basic test benches and to develop complete verification environment using System Verilog. You will also get exposure to Universal Verification Methodology (UVM). The course will conclude with an industry oriented project work.

Resource Persons:

1.Ms.M.Jasmin

2.Ms.E.Kanniga

3. Ms.S.Saravana Selvi

Convener:

Dr.M.Sundararajan

HOD/ECE

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CIRCULAR

SCHOOL OF ELECTRICAL ENGINEERING

Date: 20.08.2020

The course on Advanced Digital Logic Verificationis planned by School of Electrical Engineering which commences on 12-09-2020 (Saturday).In this regard the students are requested to give their willingness to Course Coordinator.It is instructed to actively participate and get benefitted for the certified course.

Course Coordinator: K.Subbulakshmi
Contact No:7358747803
Email id: subbulakshmi.ece@bharathuniv.ac.in

(Dr.M.Sundararajan)
HOD/ECE

To,
Copy to ECE Department,
Copy to EEE Department,
Department Notice Board

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SCHOOL OF ELECTRICAL ENGINEERING

Advanced Digital Logic Verification

SCHEDULE

Contact Hours : 31 hrs

DATE	SESSION	Contact Hours	TOPICS	Resource person
12-09-2020	FN	9.0 m to 12.30 pm	Introduction to verification concepts	Ms.E.Kanniga
	AN	1.30 pm to 4 pm	Portable Stimulus basics	Ms.S.Saravana Selvi
14-09-2020	FN	9.00 am to 12.30 pm	Data transfer synchronization between components	Ms.E.Kanniga
	AN	1.30 pm to 4 pm	Race Condition	Ms.S.Saravana Selvi
15-09-2020	FN	9.00 am to 12.30 pm	Meta stability	Ms.E.Kanniga
	AN	1.30 pm to 4 pm	Power management in soc	Ms.M.Jasmin
16-09-2020	FN	9.00 am to 12.30 pm	FIFO	Ms.M.Jasmin
	AN	1.30 pm to 4 pm	State machines Registers Memories Synthesis	Ms.S.Saravana Selvi
17-09-2020	FN	9.00 am to 12.30 pm	Predict design output Gate level simulation Debugging incorrect designs	Ms.M.Jasmin
	AN	1.30 pm to 5 pm	Active low and active high PISO, SIPO Comparator	Ms.S.Saravana Selvi

VALUE ADDED COURSE

SCHOOL OF ELECTRICAL ENGINEERING

Advanced Digital Logic Verification

List of Participants

Date: 12.09.2020

Sl.no	REG.N0	NAME OF THE CANDIDATE
1	U13EC001	ABINAYA P
2	U13EC002	AKHIRUL ISLAM
3	U13EC003	ANAND RAHUL
4	U13EC005	ANJALI KUMARI
5	U13EC010	BABLOO KUMAR
6	U13EC012	CLIFFORD JOSEPH A
7	U13EC013	DAMODARAN M
8	U13EC016	DEEPSHIKHA KUMARI
9	U13EC017	DEVENDRA PRIYANKA SUNDER
10	U13EC018	ELVIS RYNTONG
11	U13EC021	JAYED AHMED LASKAR
12	U13EC023	KUMARI PRIYANKA
13	U13EC026	NABIL NAIDU S
14	U13EC027	NADAR PAVITRA KESHAVAN
15	U13EC028	NAVEEN KANNAN N
16	U13EC029	NIRAJ KUMAR
17	U13EC033	RAKESH V
18	U13EC034	RAMYA S

19	U13EC038	SHRUTHI T S
20	U13EC039	SHUBHAM KUMAR
21	U13EC040	SUKANTO SHARAN
22	U13EC041	THIYAGARAJAN V
23	U13EC047	ZAHID AHMED
24	U13EC048	BHUVANAPRIYA R
25	U13EC049	RITESH KUMAR
26	U13EC051	LAICHIMA BRAHMA
27	U13EC503	M AKSHAY REDDY
28	U13EC504	VIGNESH M
29	U13EC507	THAMIZH THENDRAL R
30	U13EC511	VIGNESH M
31	U13EC515	R NARAHARIPRUTHVIRAJU
32	U13EC517	SUBIN JERALD P
33	U13EC702	SUGENTHAN .T
34	U13EC703	UDHAYAN E K
35	U13EC705	JAI SHANKAR M
36	U13EC706	ABHISHEK PAUL
37	U13EC707	SRIJAN KUMAR
38	U13EC708	S SADHANA
39	U13EC710	KARTHIKEYAN .M
49	U13EC510	POSANI DIVYA TEJA
41	U13EC512	PRAVIN K
42	U13EC513	CHRISTOPHER EDWARD J
43	U13EC514	ANUPKUMAR L
44	U13EC571	PRAVEEN KUMAR H

45	U13EC706	ABHISHEK PAUL
46	U13EC006	ARAVIND V
47	U13EC008	ASHIQUE ALAM
48	U13EC009	ASHVATHAMAN K
49	U13EC019	G RAHUL REDDY
50	U13EC020	ISWARYA S
51	U13EC030	P PRAVEEN
52	U13EC031	PRAVEEN KUMAR V
53	U13EC032	RAHUL KUMAR
54	U13EC042	UTTAM KUMAR
55	U13EE003	ALOK KUMAR
56	U13EE005	ASHISH KUMAR YADAV

(Dr.M.Sundararajan)

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SCHOOL OF ELECTRICAL ENGINEERING

VALUE ADDED COURSE

Advanced Digital Logic Verification

FEED BACK FORM					Date:17.9.2020
Name	Alok Kumar				
	Poor	Fair	Good	Very Good	Excellent
Overall Program				✓	
TheSpeaker				✓	
Audio,Visual Aids Technology used					✓
Presentation hand outs				✓	

Student Signature

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NAAC

ABET

SCHOOL OF ELECTRICAL ENGINEERING

CERTIFICATE OF PARTICIPATION

This is to certify that Mr/Ms. **ABINAYA P** has attended Value added Course on "**Advanced Digital Logic Verification** " Organized by the school of Electrical Engineering, BIHER conducted from 12-09-2020 to 17-09-2020.

Ms. K.Subbulakshmi
COURSE COORDINATOR

Dr. M. Sundararajan
CONVENOR